Letters

Minimization of DC-Bus Current Ripple in Modular Multilevel Converter Under Unbalanced Conditions

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***Abstract*—In a modular multilevel converter (MMC), the zero-sequence currents at twice the fundamental frequency and its multiples flow through the dc bus and cause dc-bus power fluctuations during unbalanced conditions. These fluctuations appear in dc-bus current, considering that the dc-bus voltage is stiff. In this paper, a model-predictive control is proposed to minimize the ripple in dc-bus current. The proposed approach takes the advantage of internally generated zero-sequence voltage to mitigate the zero-sequence current during unbalanced conditions. To implement the proposed approach, a generalized mathematical model of the MMC, which includes the zero-sequence voltage, is presented. The performance of the proposed approach is verified through MATLAB/Simulink simulations on a 4.16-kV/5-MW system and dSPACE/DS1103-based experiments on a 208-V/3-kW laboratory prototype.**

***Index Terms*—DC-bus current ripple, model-predictive control (MPC), modular multilevel converter (MMC), zero-sequence voltage.**

I. Introduction

THE circulating current control is one of the major challenges in a modular multilevel converter (MMC). During unbalanced operation, the circulating current consists of zero-sequence components along with the positive- and negative-sequence components at twice the line frequency [1]. The positive- and negative-sequence circulating current flows among the converter legs. On the contrary, the zero-sequence circulating current flows through the dc bus and converter legs, leading to a ripple in dc-bus power. These ripples appear in dc-bus current, considering that the dc-bus voltage is maintained stiff [1]. The dc-bus current ripple increases the ripple in submodule capacitor voltage and the magnitude of the arm current, which has a cascaded effect on the semiconductor device voltage stress and conduction losses [1].

The classical control methods use proportional–integral regulators in synchronous dq frame or proportional–resonant regulators in stationary $\alpha\beta$ frame to control the zero-sequence circulating currents [2]. Alternatively, the dc-bus current or submodule capacitor voltage ripple is directly controlled by using resonant regulators; therefore, the magnitude of zero-sequence currents is minimized [3]–[5]. The performance of classical control methods greatly depends on the controller bandwidth and switching frequency [6], [7]. In addition, the reference frame transformation is required to extract the zero-sequence currents in classical control methods.

On the other hand, the model-predictive control (MPC) approach overcomes the drawbacks of classical control methods and improves the performance of the MMC. The effectiveness of the MPC approach is presented under balanced conditions only, where the negative-sequence circulating currents are effectively controlled using a cost function [8]. Several MPC methods focusing on reduction of computational complexity, harmonic distortion, and current ripple under balanced operating conditions are presented [9], [10]. However, there are no studies about the minimization of dc-bus current ripple or zero-sequence circulating currents during unbalanced conditions using the MPC approach.

This paper proposes a three-phase MPC approach to mitigate the dc-bus current ripple during unbalanced conditions. To implement the proposed approach, a generalized discrete-time model of an MMC is presented. The system model includes the zero-sequence voltage, which modifies the switching pattern of upper and lower arms. The modified switching pattern generates a zero-sequence voltage along with the fundamental frequency voltage across the arms. The zero-sequence voltage minimizes the magnitude of zero-sequence currents, which further reduces the ripple in dc-bus current. The performance of the proposed approach is validated through the MATLAB simulations and dSPACE-DS1103 experiments on a laboratory prototype. The main contributions of this paper are highlighted as follows:

1) a generalized three-phase mathematical model of an MMC, which includes the zero-sequence voltage, is presented;
2) minimization of the ripple in dc-bus current during unbalanced conditions is addressed;
3) minimization of circulating currents is proposed, such that the peak and root-mean-square value of arm currents are kept within the limits;

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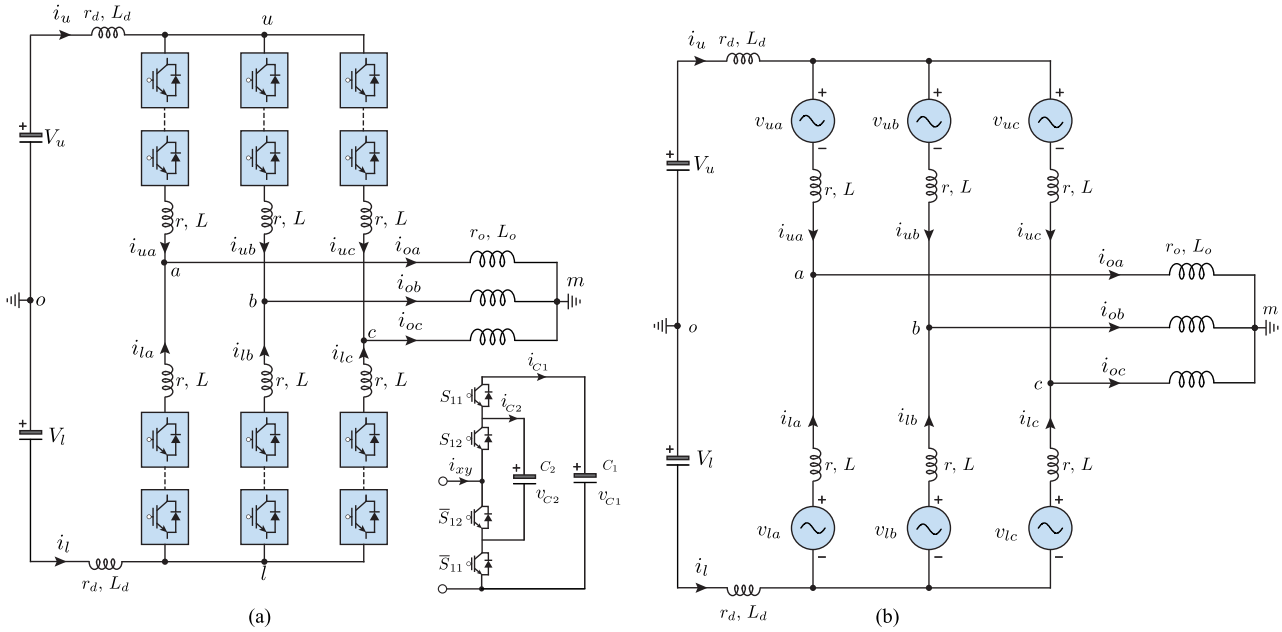

Fig. 1. (a) Configuration of a three-phase MMC and 3L-FC submodule. (b) Equivalent model of a three-phase MMC.

4) minimization of the ripple in submodule capacitors voltage during unbalanced conditions is studied;
5) voltage and current harmonic distortion is reduced.

II. Generalized Mathematical Model of MMC

The structure of a three-phase MMC connected to a simple passive load is shown in Fig. 1(a). The MMC consists of N submodules in series with an inductor L in each arm. The power losses in the inductor are represented with a resistor r. The N submodules are modeled as a controlled voltage source $v_{\rm xy}$, as shown in Fig. 1(b), where $x \in \{u, l\}$ represents the arm and $y \in \{a, b, c\}$ represents the phase. The dc system is connected across converter legs through a dc inductor L_d and its internal resistance r_d. The dc system is represented with a split dc voltage source of V_u and V_l, where $V_u = V_l = \frac{V_d}{2}$. The ac system of the MMC is connected to an inductance L_o and resistance r_o in star configuration.

To analyze the dynamic behavior of the MMC, the common-mode current ($i_{\rm cm}$), dc current (i_d), ac circulating current ($i_{\rm xz}$), and ac output current (i_x) components are considered in the arm current ($i_{\rm xy}$). From the equivalent model shown in Fig. 1(b), the upper and lower arm currents of phase a are given by

$$\begin{aligned} i_{\rm ua} &= i_{\rm cm} + i_a + i_d + i_{\rm az} \\ i_{\rm la} &= i_{\rm cm} + i_a - i_d - i_{\rm az}. \end{aligned} \tag{1}$$

The current flowing through the upper and lower dc bus of the MMC is given by

$$\begin{aligned} i_u &= i_{\rm ua} + i_{\rm ub} + i_{\rm uc} = 3\,i_{\rm cm} + 3\,i_d \\ i_l &= i_{\rm la} + i_{lb} + i_{lc} = 3\,i_{\rm cm} - 3\,i_d. \end{aligned} \tag{2}$$

Similarly, the ac output current flowing through phase a of passive load and the common-mode current are formulated as follows:

$$\begin{aligned} i_{\rm oa} &= 2\,i_a + 2\,i_{\rm cm} \\ i_{\rm cm} &= \frac{i_u + i_l}{6}. \end{aligned} \tag{3}$$

From the equivalent model shown in Fig. 1(b), the voltage equations of phase a, upper and lower arms, are given as

$$\left.\begin{aligned} V_u &= L_d \frac{d\,i_u}{dt} + r_d\,i_u + v_{\rm ua} + L\frac{d\,i_{\rm ua}}{dt} \\ &\quad + r\,i_{\rm ua} + L_o\frac{d\,i_{\rm oa}}{dt} + r_o\,i_{\rm oa} \\ -V_l &= L_d \frac{d\,i_l}{dt} + r_d\,i_l - v_{\rm la} + L\frac{d\,i_{\rm la}}{dt} \\ &\quad + r\,i_{\rm la} + L_o\frac{d\,i_{\rm oa}}{dt} + r_o\,i_{\rm oa}. \end{aligned}\right\} \tag{4}$$

The summation of phase a, upper and lower arm, voltages in (4) gives the following equation:

$$\begin{aligned} 0 &= L_d \frac{d\,(i_u + i_l)}{dt} + r_d\,(i_u + i_l) + v_{\rm ua} - v_{\rm la} \\ &\quad + L\frac{d\,(i_{\rm ua} + i_{\rm la})}{dt} + r\,(i_{\rm ua} + i_{\rm la}) \\ &\quad + 2L_o\frac{d\,i_{\rm oa}}{dt} + 2r_o\,i_{\rm oa}. \end{aligned} \tag{5}$$

Substituting (3) into (5) results in

$$\begin{aligned} 0 &= 6L_d \frac{d\,i_{\rm cm}}{dt} + 6r_d\,i_{\rm cm} + v_{\rm ua} - v_{\rm la} + 2L\frac{d\,i_{\rm cm}}{dt} \\ &\quad + 2r\,i_{\rm cm} + 2L\frac{d\,i_a}{dt} + 2r\,i_a + 4L_o\frac{d\,i_{\rm cm}}{dt} \\ &\quad + 4r_o\,i_{\rm cm} + 4L_o\frac{d\,i_a}{dt} + 4r_o\,i_a. \end{aligned} \tag{6}$$

Similarly, the phase b and phase c voltage equations are given by

$$\left.\begin{aligned} 0 &= 6L_d\,\frac{d\,i_{\rm cm}}{dt} + 6r_d\,i_{\rm cm} + v_{\rm ub} - v_{lb} + 2L\,\frac{d\,i_{\rm cm}}{dt} \\ &\quad + 2r\,i_{\rm cm} + 2L\,\frac{d\,i_b}{dt} + 2r\,i_b + 4L_o\,\frac{d\,i_{\rm cm}}{dt} \\ &\quad + 4r_o\,i_{\rm cm} + 4L_o\,\frac{d\,i_b}{dt} + 4r_o\,i_b \\ 0 &= 6L_d\,\frac{d\,i_{\rm cm}}{dt} + 6r_d\,i_{\rm cm} + v_{\rm uc} - v_{lc} + 2L\,\frac{d\,i_{\rm cm}}{dt} \\ &\quad + 2r\,i_{\rm cm} + 2L\,\frac{d\,i_c}{dt} + 2r\,i_c + 4L_o\,\frac{d\,i_{\rm cm}}{dt} \\ &\quad + 4r_o\,i_{\rm cm} + 4L_o\,\frac{d\,i_c}{dt} + 4r_o\,i_c. \end{aligned}\right\} \tag{7}$$

The dynamic model of common-mode current is obtained by adding (6) and (7) as

$$\frac{d\,i_{\rm cm}}{dt} = \frac{1}{3L_d + L + 2L_o}\Big[\underbrace{\sum_{x=a,b,c}\frac{v_{\rm lx} - v_{\rm ux}}{6}}_{\text{Zero-Sequence Voltage}} - (3r_d + r + 2r_o)\,i_{\rm cm}\Big]. \tag{8}$$

A. Modeling of AC Output Current

The ac output current is equally distributed among the upper and lower arms. From (1), the magnitude of phase a ac output current is given by

$$i_a = \frac{i_{\rm ua} + i_{\rm la}}{2} - i_{\rm cm}. \tag{9}$$

The dynamic model of phase a ac output current is obtained by solving (6), (8), and (9) as

$$\frac{d\,i_a}{dt} = \frac{1}{L + 2L_o}\left[\frac{v_{\rm la} - v_{\rm ua}}{2} - \underbrace{\sum_{x=a,b,c}\frac{v_{\rm lx} - v_{\rm ux}}{6}}_{\text{Zero-Sequence Voltage}} - (r + 2r_o)\,i_a\right]. \tag{10}$$

From (10), the generalized dynamic model of three-phase ac output currents is developed as

$$\frac{d\,\mathbf{i_x}}{dt} = \frac{1}{L + 2L_o}\left[\frac{\mathbf{v_{lx}} - \mathbf{v_{ux}}}{2} - \underbrace{\sum_{x=a,b,c}\frac{v_{\rm lx} - v_{\rm ux}}{6}}_{\text{Zero-Sequence Voltage}} - (r + 2r_o)\,\mathbf{i_x}\right]. \tag{11}$$

The continuous-time model given in (11) is transformed into the discrete-time domain using forward Euler approximation as follows:

$$\mathbf{i_x^p}(k+1) = \Gamma_o\left[\frac{\mathbf{v_{lx}^p}(k) - \mathbf{v_{ux}^p}(k)}{2} - \underbrace{\sum_{x=a,b,c}\frac{v_{\rm lx}^p(k) - v_{\rm ux}^p(k)}{6}}_{\text{Zero-Sequence Voltage}}\right] + \Phi_o\,\mathbf{i_x^m}(k) \tag{12}$$

where

$$\Gamma_o = \frac{T_s}{L + 2L_o}, \quad \Phi_o = 1 - \frac{(r + 2r_o)\,T_s}{L + 2L_o}. \tag{13}$$

The zero-sequence voltage term in (11) is used to minimize the dc-bus current ripple in the MMC during unbalanced operating conditions.

B. Modeling of Arm Voltage

The MMC is constructed using a three-level flying capacitor (3L-FC) submodule, as shown in Fig. 1(a). The 3L-FC submodule has two floating capacitors C_1 and C_2 with a voltage of v_{C1} and v_{C2}, respectively. The voltage equations of capacitors C_1 and C_2 in continuous time are given as follows:

$$\left.\begin{aligned} v_{C1}(t) &= v_{C1}(0) + \frac{1}{C_1}\int_{0+}^{t} i_{C1}(\tau)\,d\tau \\ v_{C2}(t) &= v_{C2}(0) + \frac{1}{C_2}\int_{0+}^{t} i_{C2}(\tau)\,d\tau \end{aligned}\right\} \tag{14}$$

where $v_{C1}(0)$ and $v_{C2}(0)$ represent the initial voltages of capacitors C_1 and C_2, respectively. i_{C1} and i_{C2} represent the currents flowing through capacitors C_1 and C_2, respectively.

The voltage equations of capacitors C_1 and C_2 in discrete time are given by

$$\left.\begin{aligned} v_{C1}^p(k+1) &= v_{C1}^m(k) + \frac{T_s}{C_1} i_{C1}^p(k) \\ v_{C2}^p(k+1) &= v_{C2}^m(k) + \frac{T_s}{C_2} i_{C2}^p(k). \end{aligned}\right\} \tag{15}$$

The capacitor current is formulated in terms of switching states and arm current as follows:

$$\left.\begin{aligned} i_{C1}^p(k) &= S_{11}^p(k)\,i_{\rm xy}^m(k) \\ i_{C2}^p(k) &= (S_{12}^p(k) - S_{11}^p(k))\,i_{\rm xy}^m(k). \end{aligned}\right\} \tag{16}$$

The submodule output voltage is given by

$$v_{M1}^p(k) = S_{11}^p\,v_{C1}^m(k) + (S_{12}^p - S_{11}^p)\,v_{C2}^m(k) \tag{17}$$

where $v_{C1}^m(k)$ and $v_{C2}^m(k)$ are the measured voltages.

Each arm consists of N submodules. The summation of output voltages in N submodules gives the arm voltage

$$v_{\rm xy}^p(k) = v_{M1}^p(k) + v_{M2}^p(k) + \cdots + v_{MN}^p(k). \tag{18}$$

III. Design Steps of MPC

The implementation of MPC involves various stages, such as generation of reference currents, extrapolation of reference cur-

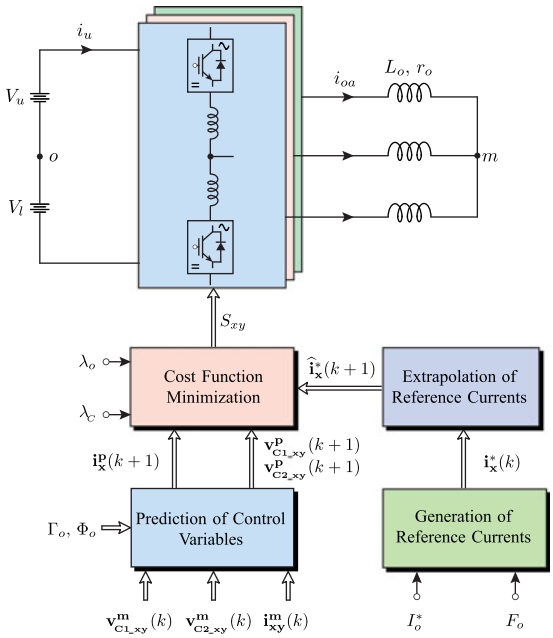

Fig. 2. Block diagram MPC for a three-phase MMC.

rents, prediction of control variables, formulation of cost function, and identification of optimal switching state, as shown in Fig. 2. In this study, the reference currents are generated in open loop corresponding to the required magnitude and frequency. The complete design steps of MPC are given as follows.

1) Measure the three-phase arm currents $\mathbf{i}^{\mathbf{m}}_{\mathbf{xy}}(k)$ and submodule capacitors voltage $\mathbf{v}^{\mathbf{m}}_{\mathbf{C1\_xy}}(k)$ and $\mathbf{v}^{\mathbf{m}}_{\mathbf{C2\_xy}}(k)$.
2) Predict the submodule capacitors voltage $\mathbf{v}^{\mathbf{p}}_{\mathbf{C1\_xy}}(k+1)$ and $\mathbf{v}^{\mathbf{p}}_{\mathbf{C2\_xy}}(k+1)$ using (15) and (16).
3) Predict the future behavior of the arm voltages $\mathbf{v}^{\mathbf{p}}_{\mathbf{xy}}(k)$ by using (17) and (18).
4) Predict $\mathbf{i}^{\mathbf{p}}_{\mathbf{x}}(k+1)$ using (12) and (13).
5) Generate reference currents $\mathbf{i}^*_{\mathbf{x}}(k)$ for a peak value of I^*_o and fundamental frequency F_o. Extrapolate kth instant ac output currents to $(k+1)$th instant by using a third-order Lagrange extrapolation technique given below:

$$\hat{\mathbf{i}}^*_{\mathbf{x}}(k+1) = 4\mathbf{i}^*_{\mathbf{x}}(k) - 6\mathbf{i}^*_{\mathbf{x}}(k-1) + 4\mathbf{i}^*_{\mathbf{x}}(k-2) - \mathbf{i}^*_{\mathbf{x}}(k-3). \quad (19)$$

6) Set the nominal voltage of submodule capacitors C_1 and C_2 to $\mathbf{v}^*_{\mathbf{C1\_xy}}(k+1) = \frac{V_d}{N}$ and $\mathbf{v}^*_{\mathbf{C2\_xy}}(k+1) = \frac{V_d}{2N}$, respectively.
7) Formulate a cost function by incorporating the reference variables $\mathbf{i}^*_{\mathbf{x}}(k+1)$, $\mathbf{v}^*_{\mathbf{C1\_xy}}(k+1)$, and $\mathbf{v}^*_{\mathbf{C2xy}}(k+1)$, and predicted control variables $\mathbf{i}^{\mathbf{p}}_{\mathbf{x}}(k+1)$, $\mathbf{v}^{\mathbf{p}}_{\mathbf{C1\_xy}}(k+1)$, and $\mathbf{v}^{\mathbf{p}}_{\mathbf{C2xy}}(k+1)$:

$$g(k) = \lambda_o \times |\mathbf{i}^*_{\mathbf{x}}(k+1) - \mathbf{i}^{\mathbf{p}}_{\mathbf{x}}(k+1)| + \lambda_C \times |\mathbf{v}^*_{\mathbf{C1\_xy}}(k+1) - \mathbf{v}^{\mathbf{p}}_{\mathbf{C1\_xy}}(k+1)| + \lambda_C \times |\mathbf{v}^*_{\mathbf{C2\_xy}}(k+1) - \mathbf{v}^{\mathbf{p}}_{\mathbf{C2\_xy}}(k+1)| \quad (20)$$

where λ_o and λ_C represent the weight factors of the ac output current and submodule capacitor voltage control, respectively.

IV. Simulation and Experimental Validation

A. Simulation Validation

The performance of the proposed approach is verified on a three-phase MMC with two 3L-FC submodules/arm. Each submodule capacitors have nominal voltage of $V_{C1} = 3.677$ kV and $V_{C2} = 1.838$ kV. In this study, the comparison of the proposed MPC and existing standard MPC approaches is presented. In standard MPC, each phase of the MMC is controlled using an independent predictive controller. The per-phase discrete-time model given in (21) is used to implement the standard MPC [11]

$$\mathbf{i}^{\mathbf{p}}_{\mathbf{x}}(k+1) = \Gamma_o\,[\mathbf{v}^{\mathbf{p}}_{\mathbf{lx}}(k) - \mathbf{v}^{\mathbf{p}}_{\mathbf{ux}}(k)] + \Phi_o\,\mathbf{i}^{\mathbf{m}}_{\mathbf{x}}(k). \quad (21)$$

The performance of the standard MPC is shown in Fig. 3(a), where the phase a and phase c reference currents are generated with a peak value of 0.6 p.u. and a frequency of 60 Hz. The phase b reference current is generated with a 20% unbalance in the magnitude as that of other phases. The actual output currents perfectly follow their reference currents, as shown in (i) in Fig. 3(a). The unbalanced operation leads to an asymmetrical nature of arm currents, as shown in (ii) in Fig. 3(a), which leads to an asymmetrical nature of ac circulating currents. The ac circulating current consists of zero-sequence current components along with the positive- and negative-sequence components. The zero-sequence circulating current at twice the fundamental frequency and its multiples flows through the dc bus and causes a significant ripple in dc-bus current, as shown in (iii) in Fig. 3(a). The second harmonic component is the dominant component and has a magnitude of 59.31 A along with other harmonic components. The dc-bus current ripple also increases the magnitude of circulating currents, as shown in (iv) in Fig. 3(a), which further increases the device power losses and effects the system efficiency.

The performance of the proposed approach is shown in Fig. 3(b), under identical operating conditions as that of standard MPC. The proposed approach generates a zero-sequence voltage along with the fundamental voltage across the arm. The fundamental voltage forces the fundamental frequency current component corresponding to the reference current, as shown in (i) in Fig. 3(b). The zero-sequence voltage blocks the zero-sequence circulating currents flowing through the dc bus and converter legs. Therefore, the magnitude of arm currents is kept within the limits, as shown in (ii) in Fig. 3(b). The dc-bus current has a second harmonic component of 16.71 A, which is reduced by 71.8% in comparison to the standard MPC. Thereby, the fluctuations in dc-bus current are minimized, as shown in (iii) in Fig. 3(b), which further reduces the magnitude of circulating currents, as shown in (iv) in Fig. 3(b). The reduction of ac circulating current improves the system efficiency.

B. Experimental Validation

The simulation study is validated on a dSPACE-DS1103-based MMC laboratory prototype. Each converter leg has two 3L-FC submodules with a nominal voltage of $V_{C1} = 360$ V and $V_{C2} = 180$ V. The phase a and phase c reference currents are generated for a peak value of 13 A and a frequency of 60 Hz. The phase b reference current is generated with a 20% unbalance in

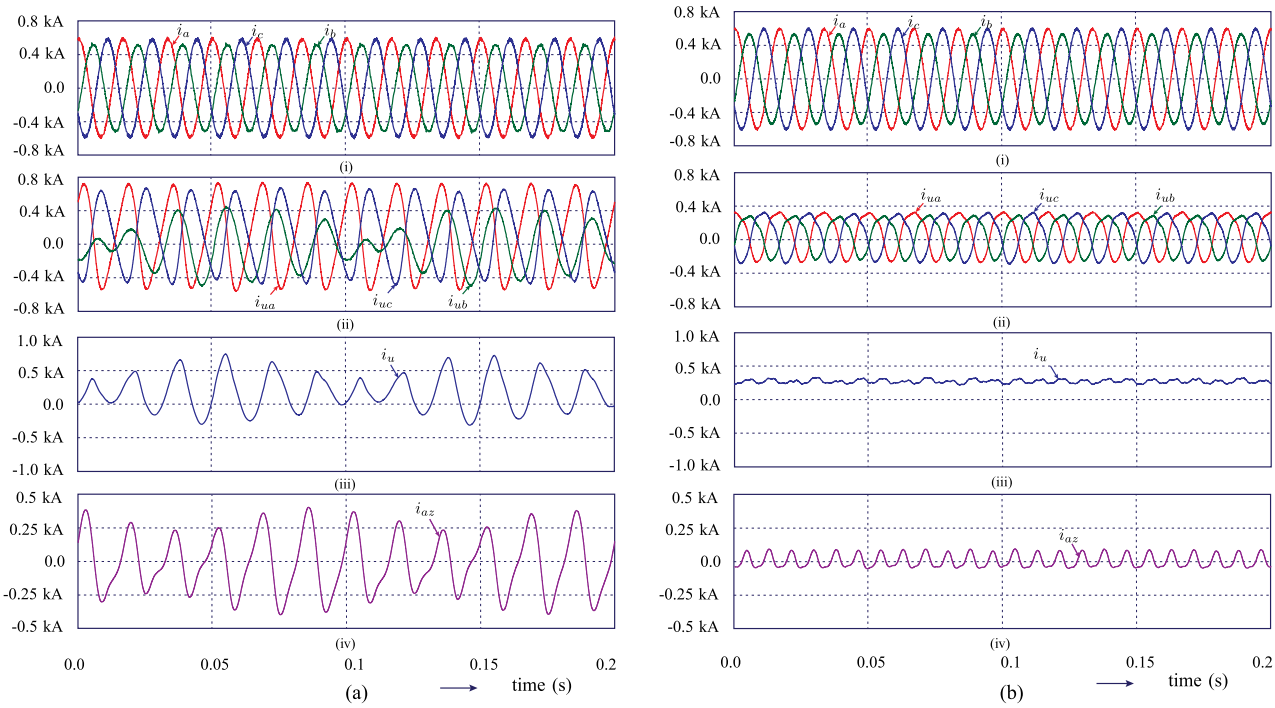

Fig. 3. Simulation results. (a) Standard MPC. (b) Proposed MPC. [(i) output currents, (ii) upper arm currents, (iii) dc-bus current, and (iv) circulating current.]

TABLE I
PERFORMANCE COMPARISON OF THE STANDARD AND PROPOSED MPC

Performance Indices	Standard MPC	Proposed MPC
I_{THD}	4.94%	3.42%
i_u (Zero-Sequence Current)	0.336 A	0.21 A
V_{C1} Ripple (p-p)	16 V	12 V
V_{C2} Ripple (p-p)	8 V	5 V
CC (rms)	7.15 A	6.91 A
V_{THD}	36.65%	25.23%
CMV (p-p)	360 V@ 60 Hz	360 V@ 180 Hz

TABLE II
ZERO-SEQUENCE CURRENT COMPONENTS IN DC-BUS CURRENT

Harmonic Component	Standard MPC	Proposed MPC
Second Harmonic	0.57 A	0.21 A
Fourth Harmonic	0.4 A	0.14 A
Sixth Harmonic	0.73 A	0.57 A

magnitude. With the standard MPC, the actual currents follow their reference currents, as shown in (i) in Fig. 4(a). These currents are nonsinusoidal in nature with a harmonic distortion of 4.94%, as shown in Table I. The zero-sequence current components in dc-bus current are summarized in Table II. The dc-bus current has a total 0.336 A of zero-sequence current component along with dc current component. The zero-sequence current increases the ripple in dc-bus current and distortion in arm currents, as shown in (ii) in Fig. 4(a). The submodule outer and inner capacitor voltages are maintained at 360 and 180 V, respectively. These capacitors have a peak–peak ripple of 16 and 8 V, as shown in Table I. Due to the zero-sequence currents, the charging and discharging of submodule capacitors in upper and lower arms are not in symmetry, as shown in (iii) in Fig. 4(a). The difference in upper and lower arm voltages causes negative-sequence circulating current, which flows among the converter legs. The phase a circulating current (includes zero-, negative-, and positive-sequence components) has a peak–peak value of 7.15 A. The standard MPC approach generates only fundamental frequency voltage across the arms, as shown in (iv) in Fig. 4(a). Therefore, the zero-sequence currents cannot be controlled with this approach. The output line voltage has a harmonic distortion of 36.65%. The voltage across the terminals m and o is around 360 V.

The performance of the proposed approach is presented in Fig. 4(b), with the above operating conditions. The proposed MPC perfectly generates three-phase sinusoidal currents with a harmonic distortion of 3.42%, as shown in (i) in Fig. 4(b), which is 30.77% smaller than that of the standard MPC. The proposed approach reduces the zero-sequence current component by 37.5%, which further minimizes the ripple in dc-bus current, as shown in (ii) in Fig. 4(b). The three-phase arm currents are balanced in nature, as shown in (ii) in Fig. 4(b). In addition, the submodule capacitor voltages in upper and lower arms are perfectly regulated at their nominal value, as shown in (iii) in Fig. 4(b). The outer and inner capacitor voltage ripple is reduced by 25% and 37.5%, respectively. This approach ensures the symmetrical charging and discharging of submodule capacitors in upper and lower arms. Therefore, the magnitude of negative-sequence circulating currents can be reduced. The circulating current has a peak–peak value of 6.91 A, as shown in (iv) in Fig. 4(b). The proposed approach generates a voltage waveform across the arm corresponding to the fundamental and zero-sequence currents, as shown in (iv) in Fig. 4(b). The zero-sequence voltage appears in the form CMV, across the terminals m and o. The CMV has a peak–peak value of 360 V.

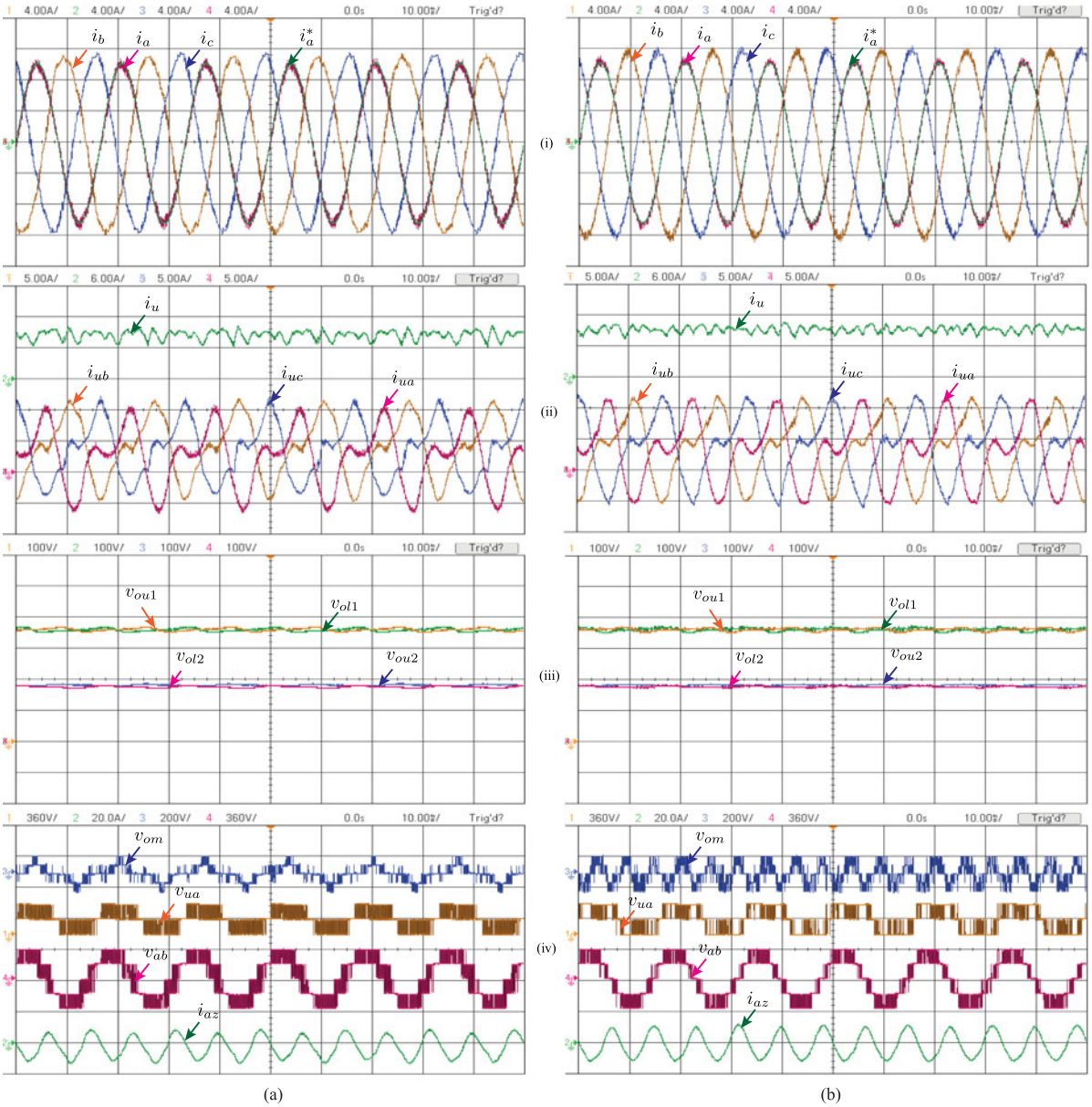

Fig. 4. Experimental results. (a) Standard MPC and (b) the proposed MPC [Scope-(i): Ch-1: actual line current i_b (5 A/div), Ch-2: reference line current i_a^* (5 A/div), Ch-3: actual line current i_c (5 A/div) and Ch-4: actual line current i_a (5 A/div). Scope-(ii): Ch-1: phase-b, upper arm current $i_{\rm ub}$ (5 A/div), Ch-2: dc-bus current i_u (6 A/div), Ch-3: phase-c, upper arm current $i_{\rm uc}$ (5 A/div), Ch-4: phase-a, upper arm current $i_{\rm ua}$ (5 A/div). Scope-(iii): Ch-1: phase-a, upper arm SM_1 capacitor voltage ($v_{\rm ou1}$) (100 V/div), Ch-2: phase-a, lower arm SM_1 capacitor voltage (v_{ol1}) (100 V/div), Ch-3: phase-a, upper arm SM_2 capacitor voltage ($v_{\rm ou2}$) (100 V/div) and Ch-4: phase-a, lower arm SM_2 capacitor voltage (v_{ol2}) (100 V/div). Scope-(iv): Ch-1: phase-a, upper arm voltage $v_{\rm ua}$ (360 V/div), Ch-2: phase-a circulating currents $i_{\rm az}$ (20 A/div), Ch-3: CMV $v_{\rm om}$ (200 V/div) and Ch-4: output line voltage $v_{\rm ab}$ (360 V/div). Time scale: 10 ms/div].

The inclusion of zero-sequence voltage in the mathematical model reduces the output line voltage harmonic distortion by 31.15%.

The switching of standard and proposed MPC approaches is analyzed experimentally. The gating signal of SM_1 with standard and proposed MPC approaches is shown in Fig. 5. With the standard MPC approach, each submodule is switched at a frequency of 3.6 kHz, as shown in Fig. 5(a). In the case of the proposed approach, each submodule is switched at a frequency of 2.2 kHz, as shown in Fig. 5(b). With the proposed approach, the submodule switching frequency is reduced by 38.88%.

V. Conclusion

In this paper, an MPC approach is proposed to minimize the ripple in dc-bus current during unbalanced conditions. To implement the proposed approach, a generalized three-phase mathematical model of an MMC is presented. The performance of the proposed MPC is compared with the standard MPC approach. The results show that the zero-sequence voltage in the proposed model blocks the zero-sequence circulating currents during unbalanced operation. Thereby, the dc-bus current ripple is minimized by 37.5% compared to the existing methodology. In addition, the proposed approach operates at the lowest

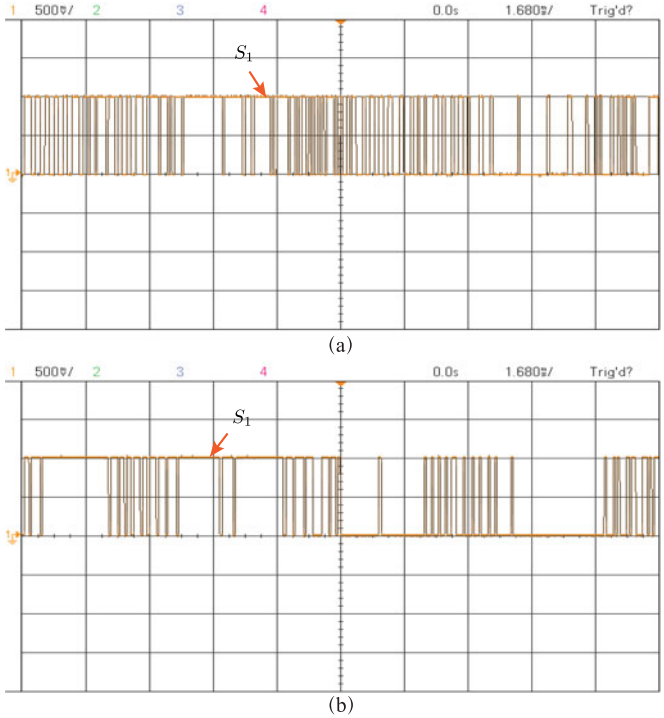

Fig. 5. Submodule switching frequency. (a) Standard MPC and (b) the proposed MPC [Scope: Ch-1: SM_1 gating signal S_1 (0.5 V/div). Time scale: 1.68 ms/div.].

switching frequency and minimizes the submodule capacitor voltage ripple and the magnitude of ac circulating currents, which improves the efficiency and reliability of the MMC. The output voltage and current waveforms are obtained with lowest harmonic distortion.

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