

An Intelligent and Efficient Fault Location and Diagnosis Scheme for Radial Distribution Systems

Seung-Jae Lee, *Member, IEEE*, Myeon-Song Choi, *Member, IEEE*, Sang-Hee Kang, *Member, IEEE*, Bo-Gun Jin, Duck-Su Lee, Bok-Shin Ahn, *Member, IEEE*, Nam-Seon Yoon, Ho-Yong Kim, and Sang-Bong Wee

Abstract—In this paper, an effective fault location algorithm and intelligent fault diagnosis scheme are proposed. The proposed scheme first identifies fault locations using an iterative estimation of load and fault current at each line section. Then an actual location is identified, applying the current pattern matching rules. If necessary, comparison of the interrupted load with the actual load follows and generates the final diagnosis decision. Effect of load uncertainty and fault resistance has been carefully investigated through simulation results that turns out to be very satisfactory.

Index Terms—Distribution system, fault diagnosis, fault location, power system protection.

I. INTRODUCTION

ELECTRIC power distribution feeders are susceptible to faults caused by a variety of situations such as adverse weather conditions, equipment failure, traffic accidents, etc. When a fault occurs on a distribution line, it is very important for the utility to identify the fault location as quickly as possible for improving the service reliability. There has been much research in the fault location problem for transmission systems. This includes a traveling wave-based scheme [1] and harmonics-based scheme [2]. The apparent impedance calculated using a fundamental component is the most widely used one [3]. A fault location in the distribution system is not an easy job due to its high complexity and difficulty caused by nonhomogeneity of line, fault resistance, load uncertainty, and phase unbalance. However, the basic approach to calculate the fault location using voltage and current measurement is still the same as the transmission system case, that is to calculate the impedance using the fundamental component [4] or harmonics [5]. An additional calculation burden like recalculation of the voltage and current at each node [4], [6], [7] is needed for the compensation of the characteristics unique to the distribution system. The fact that a distribution feeder has many branches or laterals adds to the difficulty in locating the fault since

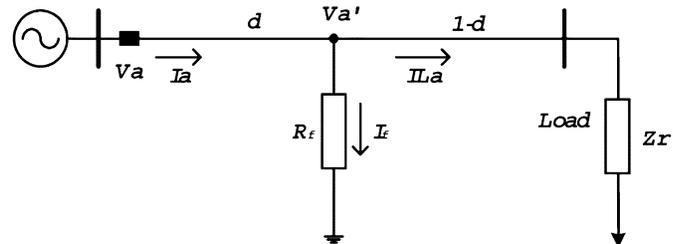


Fig. 1. Simplified distribution feeder model.

estimating the fault location based on the voltage and current signals yields more than one location. A Fuzzy approach to determine the most possible fault location is suggested [8]. In this paper, an effective fault location algorithm for the distribution feeder systems is proposed. Higher accuracy has been obtained by updating the voltage and current at the load tap or branching point of the feeder and by introducing the load estimation equation that reflects the load current change due to the voltage drop. The load uncertainty has been investigated considering various load models. This paper also proposes current pattern matching rules to determine a single fault location. A single location is identified by comparing the current pattern with the expected one due to the protective device operation during the fault. Further, the load current change, due to the circuit interruption, is utilized. Effectiveness of the proposed scheme has been proved by a number of EMTP simulations on many realistic distribution systems.

II. ITERATIVE FAULT LOCATION ALGORITHM

Consider a phase-to-ground fault on a feeder as shown in Fig. 1. The voltage measured at the incoming node is given by (1)

$$V_a = d \times (Zl_{aa}I_a + Zl_{ab}I_b + Zl_{ac}I_c) + I_f R_f \quad (1)$$

where

V_a	a-phase voltage;
I_a	a-phase current;
V'_a	a-phase voltage at fault point;
I_{La}	a-phase load current;
Z_r	equivalent load impedance matrix;
Z_l	line impedance matrix;
I_f	fault current;
R_f	fault resistance;
d	fault distance;

Manuscript received August 13, 2002. This work was supported in part by the Ministry of Science and Technology of Korea and in part by the Korea Science and Engineering Foundation through the Engineering Research Center program.

S.-J. Lee, M.-S. Choi, S.-H. Kang, and B.-G. Jin are with the Department of Electrical Engineering, Myongji University, Yongin 449-728, Korea (e-mail: sjlee@mju.ac.kr; mschoi@mju.ac.kr; shkang@mju.ac.kr; sinato@mju.ac.kr).

D.-S. Lee, B.-S. Ahn, and N.-S. Yoon are with P&C Technologies, Anyang 431-080, Korea (e-mail: fann1234@mju.ac.kr).

H.-Y. Kim is with Korea Distribution Automation System, Korea Electrotechnology Research Institute (KERI), Changwon 641-120, Korea.

S.-B. Wee is with Korea University of Technology and Education, Chonan 135-701, Korea.

Digital Object Identifier 10.1109/TPWRD.2003.820431

In case of the fault on the single-phase lateral, the voltage equation is given as

$$V_a = d \times Zl_{aa}I_a + I_f R_f. \quad (2)$$

Note that the voltage equation contains three unknown variables—fault distance (d), fault resistance (R_f), fault current (I_f). Taking the real and imaginary parts of the voltage equation and eliminating R_f , the fault distance equation can be obtained

$$d = \frac{V_{ar}I_{fi} - V_{ai}I_{fr}}{A \cdot I_{fi} - B \cdot I_{fr}} \quad (3)$$

where

$$\begin{aligned} A &= Zl_{aar}I_{ar} - Zl_{aai}I_{ai} + Zl_{abr}I_{br} - Zl_{abi}I_{bi} \\ &\quad + Zl_{acr}I_{cr} - Zl_{aci}I_{ci} \\ B &= Zl_{aar}I_{ai} + Zl_{aai}I_{ar} + Zl_{abr}I_{bi} + Zl_{abi}I_{br} \\ &\quad + Zl_{acr}I_{ci} + Zl_{aci}I_{cr}. \end{aligned}$$

Here, the subscripts (r, i) denote the real and imaginary parts. I_f can be obtained from the relation of the load current and fault current

$$I_f = I_a - I_{La}. \quad (4)$$

The load current during the fault (I_{La}) in (4) is different from the normal or prefault load current due to the voltage drop caused by the fault and it is also an unknown value. An iterative technique to estimate the load current I_{La} has been adopted and the whole fault location process is described as follows:

- i) assume I_{La} to be same as prefault load current;
- ii) find fault current I_f using (4);
- iii) determine the fault distance d using (3);
- iv) calculate the voltage at the fault using (5)

$$\begin{bmatrix} V'_a \\ V'_b \\ V'_c \end{bmatrix} = \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} - d \begin{bmatrix} Zl_{aa} & Zl_{ab} & Zl_{ac} \\ Zl_{ba} & Zl_{bb} & Zl_{bc} \\ Zl_{ca} & Zl_{cb} & Zl_{cc} \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix}; \quad (5)$$

- v) calculate the updated load current I_{La} using the voltage obtained in step iv);
- vi) go back to step ii) with new I_f and repeat the process until d converges to a certain value.

A. Load Current Estimation

Note that step v) of the fault location algorithm requires the load current calculation, which is described below.

Assuming the load has a constant impedance and its impedance is known, the load current can be calculated from (6)

$$I_{La} = [Y_{L11}, Y_{L12}, Y_{L13}] \times [V'_a, V'_b, V'_c]^T. \quad (6)$$

Here, Y_L represents the combined admittance matrix of the line section after the fault and the load in Fig. 1 and is given by

$$Y_L = [(1-d)Zl + Zr]^{-1}. \quad (7)$$

If the load impedance is not known, only the approximate load current could be estimated. Since mutual components Y_{L12}

and Y_{L13} are relatively very small compared to Y_{L11} , by neglecting them, a-phase prefault load current (I_{nLa}) is obtained by (8)

$$I_{nLa} = Y_{L11} \times V'_{na}. \quad (8)$$

Here, V'_{na} denotes the prefault voltage at the fault point and can be calculated from (9)

$$V'_{na} = V_{na} - d \times (Zl_{aa}I_{nLa} + Zl_{ab}I_{nLb} + Zl_{ac}I_{nLc}). \quad (9)$$

In this equation, a subscript n denotes “prefault” state. Then, substituting Y_{L11} from (8) into the postfault load current equation of (10)

$$I_{La} = Y_{L11} \times V'_a \quad (10)$$

post-fault load current is obtained

$$I_{La} = \left(\frac{I_{naL}}{V'_{na}} \right) \times V'_a. \quad (11)$$

Note that since this equation neglects the mutual effect, utilizing it in the fault location would cause some error.

A generalized load model [9] in (12) could also be used to estimate the load current

$$I_{La} = I_{nr} \left| \frac{V'_a}{V_n} \right|^{n_p} + jI_{ni} \left| \frac{V'_a}{V_n} \right|^{n_q} \quad (12)$$

where

- V_n prefault load voltage;
- V'_a postfault load voltage;
- I_{nr}, I_{ni} real and imaginary components of prefault load current;
- n_p, n_q load constant.

Here, the load constant is determined according to the load characteristic. For constant current load $n_p = n_q = 0$, for constant power load $n_p = n_q = -1$, and for constant impedance load $n_p = n_q = 1$. Usually the load in the distribution system has a mixed characteristic and has n_p of 1.5–2.8 and n_q of 2.5–7.0 [9], [10].

B. V, I Estimation at Line Section

If the obtained fault distance d is larger than 1, it means the fault is not in that section, but in the following section. So another fault location process should be performed for the next section using voltage and current at the incoming node for the next section. Since the voltage and current measurements are assumed available only at the substation, a way to estimate the voltage and current at the incoming node of each line section is required and described in this section.

Consider a feeder model of Fig. 2. The voltage at node $k+1$ can be obtained using (13)

$$V_{k+1} = V_k - Z_k I_k \quad (13)$$

where

- V_k voltage vector at k th node;
- Z_k impedance matrix of k th line section;
- I_k current vector of k th section;

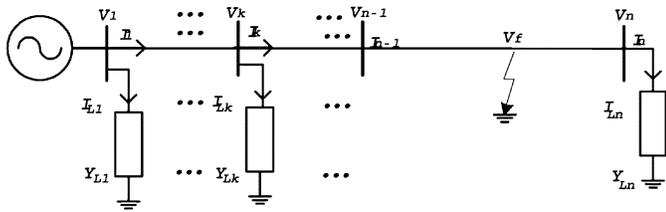


Fig. 2. Single-line feeder model.

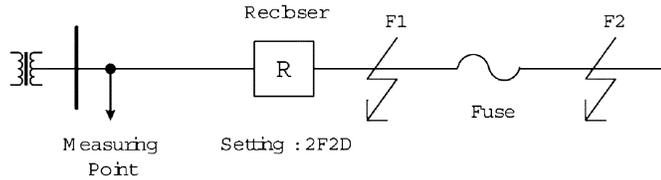


Fig. 3. Recloser-fuse line.

Assuming the constant impedance load, the current flowing out to the k th load tap can be calculated using (14)

$$I_{Lk} = V_k \times Y_{Lk} \quad (14)$$

where I_{Lk} is the load current vector of k th load tap and Y_{Lk} is the load admittance matrix at k th load tap.

The current at k th section, I_k is given as

$$I_k = I_{k-1} - I_{Lk}. \quad (15)$$

III. INTELLIGENT FAULT DIAGNOSIS

The fault diagnosis scheme proposed in this study consists of two steps: it first identifies the fault location among multiple candidate locations using current pattern information specified by the protective device operation. However, this first step could still end up with more than one location. Then, the second step attempts to diagnosis the most likely one using interrupted load information. Details of each step are described in the following sections.

A. Diagnosis Based on Current Pattern Matching

In the distribution systems, various protective devices are installed in order to protect the line, transformer, and other power equipment. Overcurrent relay, recloser, sectionalizer, and fuse are the most commonly used devices and each one has different operating characteristic. So the current pattern during the fault clearing will be subject to the device that is in charge of primary and backup protection. For example, suppose a recloser with sequence setting of 2F2D (2 fast and 2 delay operation) and fuse installed in series as shown in Fig. 3. Assume two devices are well set to satisfy the coordination. Then, for a fault F1, if all devices have operated as expected, the current measured during the fault clearing would look like Fig. 4, which shows a complete recloser operation (2 Fast and 2 Delay).

However, a fault F2 would generate the current in Fig. 5, which shows the first fast operation of the recloser and one reclosing attempt followed by the fuse blow-out during the recloser's delay operation. From this, it can be easily seen that if

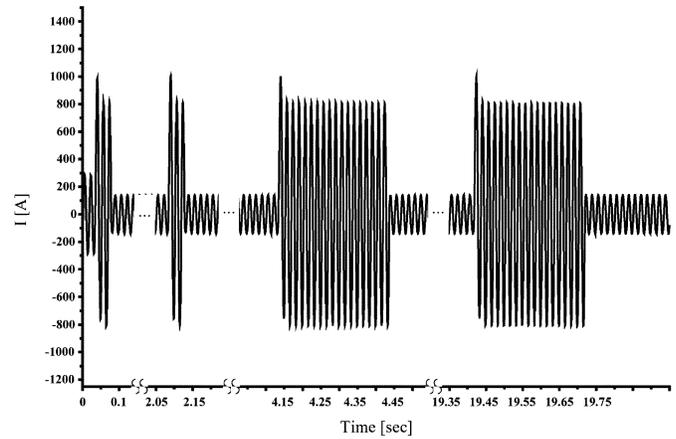


Fig. 4. Current during fault clearing by recloser.

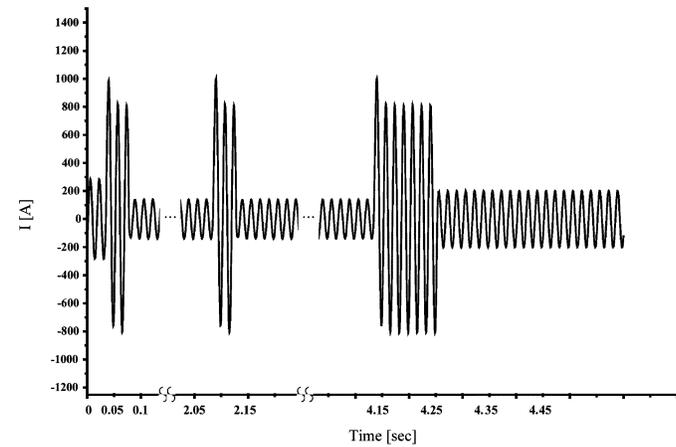


Fig. 5. Current during fault clearing by fuse.

the current waveform in Fig. 4 is given, it means F1 is the fault location. Analysis of such a current pattern could identify the protective device type involved in the fault clearing and comparing it with the protective devices that precede each fault candidate, an actual fault location can be determined.

Seven different types of protective device combinations that could precede the fault and their expected current patterns are listed in Table I. It has two columns – *device* and *conditions* and each row is the pattern identification rule that reads as “if *conditions* are met, then the preceding device is *device*.” The waveform pattern is recognized based on the number of reclosing, number of fast and delay operations. Here, the fast operation in case of the recloser represents the fault clearing within a few cycles and in case of fuse, within 20 cycles. The delay operation represents the fault clearing with more than 30 cycles. However, this criterion may vary depending on the device type and may need more investigation.

B. Diagnosis Based on Interrupted Load

Suppose preceding protective devices are same for more than one fault candidate and their corresponding current waveform patterns are the same. Then they cannot be distinguished by the rules in Table I. In this situation, a more detailed analysis on the load current before and after a fault clearing is carried out in order to diagnosis an actual fault location.

TABLE I
PATTERN IDENTIFICATION RULES

Protective Devices	Conditions
OCR	① CWF Reclosing number = OCR Reclosing number ② CWF Fast Operation number = OCR Reclosing number + 1
REC	① CWF Reclosing number = REC Reclosing number ② CWF Fast Operation number = REC Fast Operation number ③ CWF Delay Operation number = REC Delay Operation number
OCR – Fuse	① CWF Reclosing number = 0 ② CWF Fast Operation number = 1
REC – Fuse	① CWF Reclosing number = REC Fast Operation number ② CWF Fast Operation number = REC Fast Operation number + 1
Fuse – Fuse	① CWF Reclosing number = 0 ② CWF Fast Operation number = 1
REC – SEC	① CWF Reclosing number = SEC count - 1 ② CWF Fast Operation number = REC Fast Operation number ③ CWF Delay Operation number = SEC Count - REC Fast Operation number
REC - SEC – Fuse	① CWF Reclosing Operation number = REC Fast Operation number ② CWF Fast Operation number = REC Fast Operation number + 1

REC : Recloser, SEC : Sectionalizer
CWF: Current waveform.

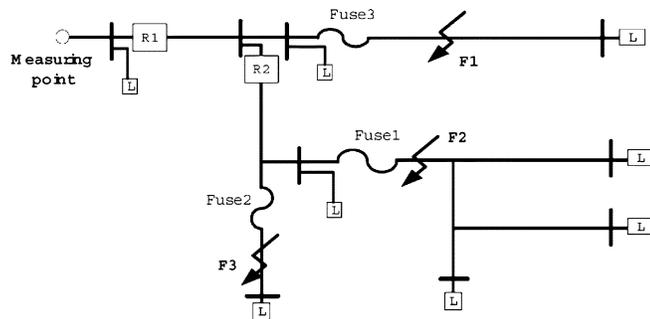


Fig. 6. Example distribution system.

Consider three fault candidates in the system shown in Fig. 6. Reclosers R1, R2 are assumed to have the same settings. Since all three faults have the same preceding protective devices, they would have the same current pattern (three “fast”) as seen in Figs. 7–9. A circuit interruption caused by recloser R1 and R2 would give different load current, which can be observed in current zone ① in the figures. It provides a clue for making a distinction among faults. Furthermore, circuit interruption by Fuse f1 and f2 would result in different line currents in zone ② and comparison of the interrupted load with the expected outage load would give additional information for the fault diagnosis.

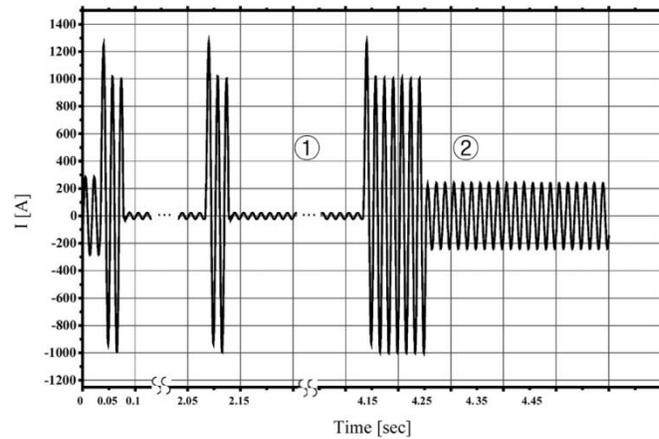


Fig. 7. Recorded current in case of fault F1.

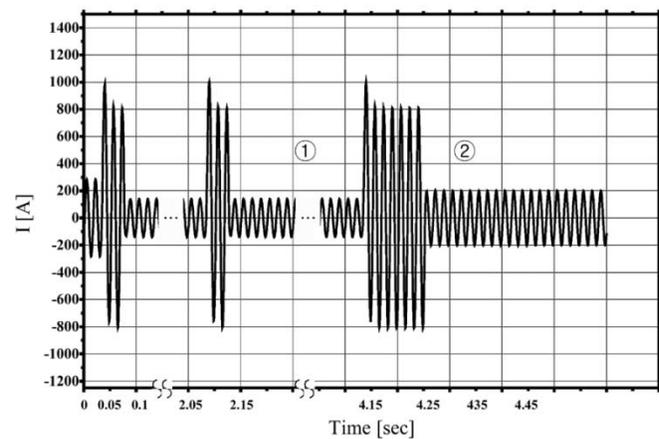


Fig. 8. Recorded current in case of fault F2.

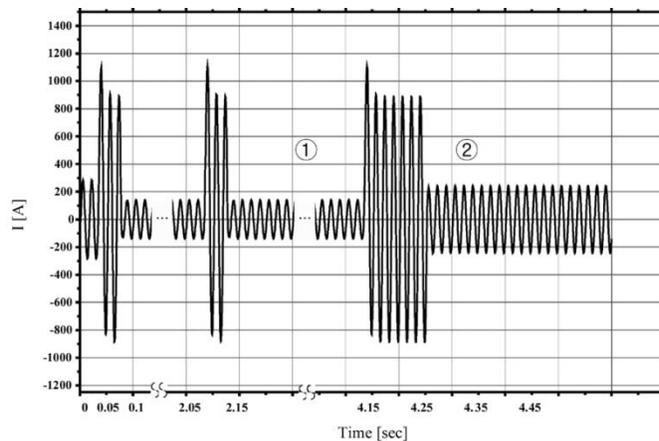


Fig. 9. Recorded current in case of fault F3.

IV. CASE STUDY

In order to show the effectiveness of the proposed algorithm, a 22.9-kV feeder in Fig. 10 is taken as a test system that has 21 nodes and single-phase and three-phase laterals. A node number is indicated along the line with its distance in parenthesis and loads (kilovolt amperes) are shown in the rectangular box. A source impedance and line impedance are shown in Table II.

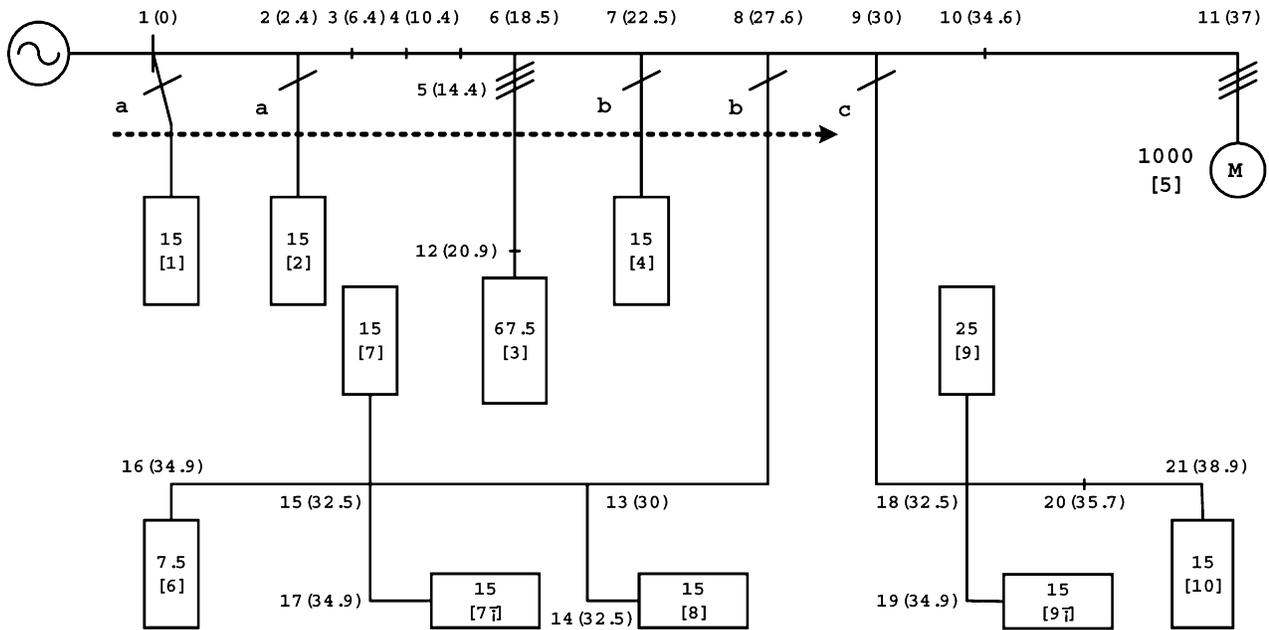


Fig. 10. Model system for fault location.

TABLE II
MODEL SYSTEM DATA

Parameters	Z1	Z0
Source [Ω]	0.094+j1.392	0.682+j2.981
Line [Ω /km]	0.56+j0.831	0.845+j2.742

TABLE III
STUDY CASES

Case	Single line to ground fault
fault distance [km]	0, 2.4, 6.4, 10.4, 14.4, 18.5, 22.5, 27.6, 30
R_f [Ω]	0, 10, 30, 50
load variation[%]	-30, 0, 30
load model	(1) Constant impedance model with known impedance (2) Constant impedance model with unknown impedance (3) Generalized model

EMTP simulations have been carried out taking ten fault locations on the thick dotted line in Fig. 10 and four fault resistance values, and adopting three different load models. The effect of the load uncertainty is also investigated by introducing average 30% variation to the load impedance used in the algorithm. Various cases that have been studied are summarized in Table III.

An estimation error of fault location is calculated using (16)

$$\%Error = \left| \frac{est.D - real.D}{total.D} \right| \times 100 \quad (16)$$

where est.D and real.D represent the estimated fault location and actual location, respectively, and total.D denotes the whole line length.

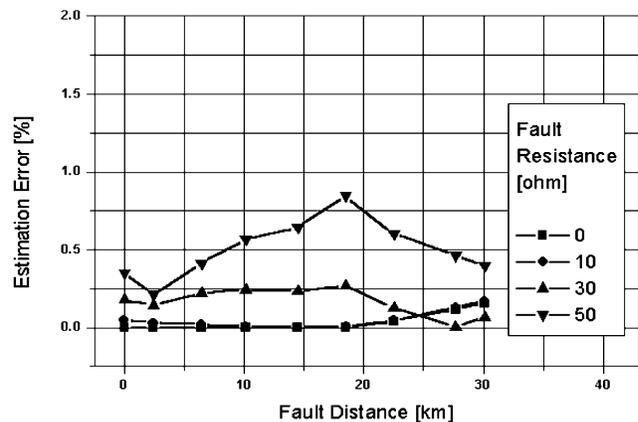


Fig. 11. Fault location error for constant impedance model with known load impedance.

A. Fault Location

1) Constant Impedance Load Model With Known Load Impedance:

a) *Effect of fault resistance:* When all loads are constant impedance type and their associated impedances are known, the proposed algorithm has generated the results summarized in Fig. 11. The maximum error of 0.6% is observed for a zero fault resistance case while the maximum error of 0.85% is observed for a fault resistance of 50 Ω . It can be seen from the figure that as the fault resistance increases, the estimation error also increases.

b) *Effect of load variation:* Figs. 12 and 13 show the fault location results when there is 30% difference between the impedance used in the algorithm and the real load impedance. It is very interesting to see that load uncertainty does not deteriorate the fault location accuracy at all showing maximum error of about 0.25% in both cases of 0- Ω and 30- Ω fault resistance. Even although taking into consideration that 30%

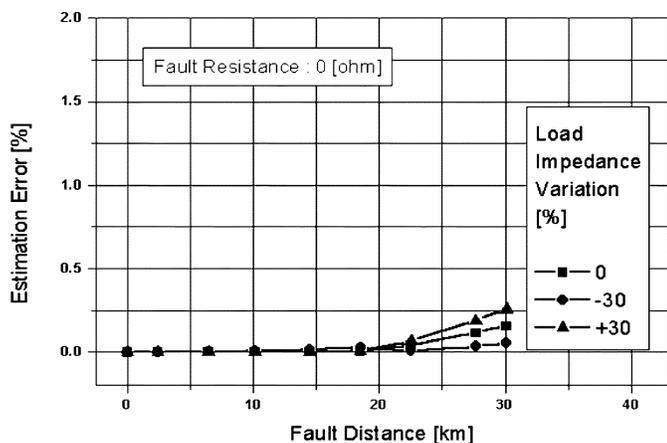


Fig. 12. Thirty-percent load variation with $R_f = 0 \Omega$.

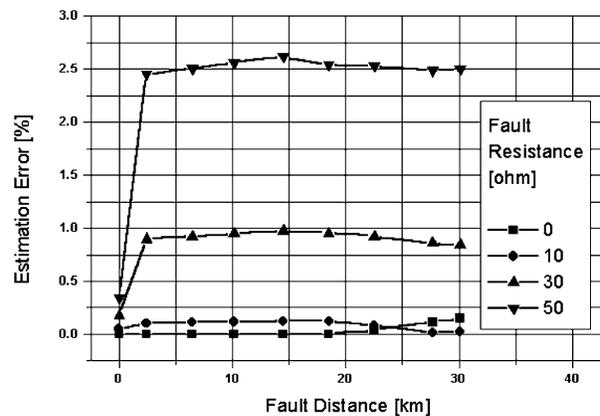


Fig. 14. Fault location error for constant impedance model with unknown load impedance.

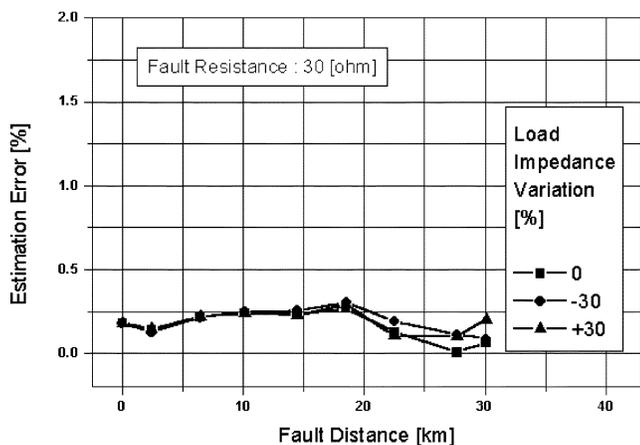


Fig. 13. Thirty-percent load variation with $R_f = 30 \Omega$.

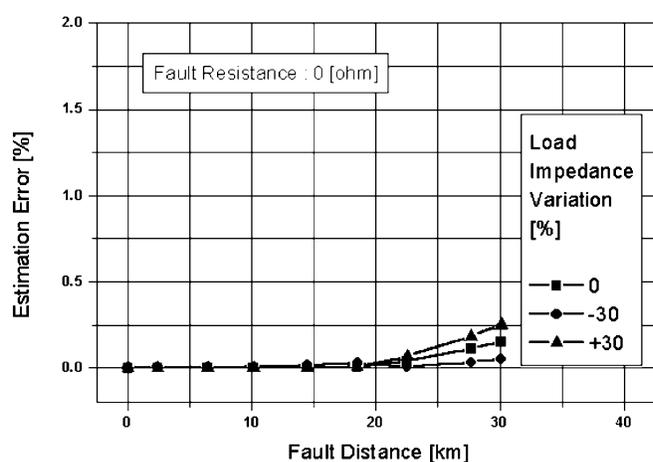


Fig. 15. Thirty-percent load variation with $R_f = 0 \Omega$.

load variation is obtained by averaging randomly generated load variation for each load by 30%, it is still a very interesting result that shows the robustness and practical power of the proposed algorithm since the exact load impedance can hardly be obtained in a real situation.

2) *Constant Impedance Load Model With Unknown Load Impedance:*

a) *Effect of fault resistance:* When the load impedance is not known for the constant impedance model, the proposed algorithm has produced the results shown in Fig. 14. It can be easily noticed that as the fault resistance increases, the estimation error also increases. The maximum error of 0.3% for a zero fault resistance case, 0.15% for 10-Ω case, 0.95% for 30-Ω case, and 2.7% for the 50-Ω case can be seen. Only the calculation error is believed to be involved in the results when the fault resistance is small.

b) *Effect of load variation:* Figs. 15 and 16 show that the effect of 30% load impedance variation is limited to only 0.25% error in case of 0-Ω fault resistance and 1.1% error in case of 30-Ω fault resistance. Again, this indicates little effect of the load variation.

3) *Generalized Load Model:*

a) *Effect of fault resistance:* A load model represented by (12) has been adopted with $n_p = 0.8$, $n_q = 1.5$, and its fault location errors for the same system are shown in Fig. 17.

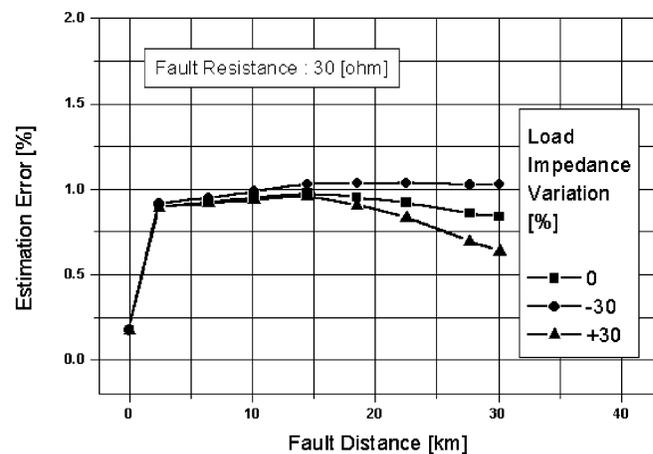


Fig. 16. Thirty-percent load variation with $R_f = 30 \Omega$.

The same observation can be made for this load model case—the bigger the fault resistance is, the higher the error is. Note that the error is limited within 2.95% for 50-Ω fault resistance. This error might be considered too big to be used for a real application. However, in all cases with less than 30-Ω fault resistance, the error is smaller than 1.0%, showing enough accuracy for a real application.

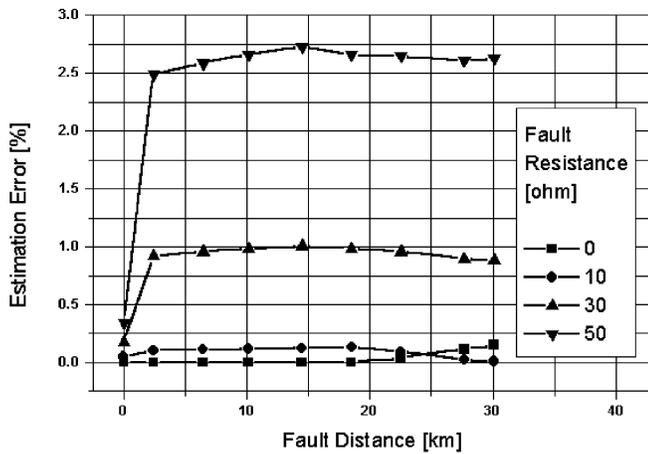
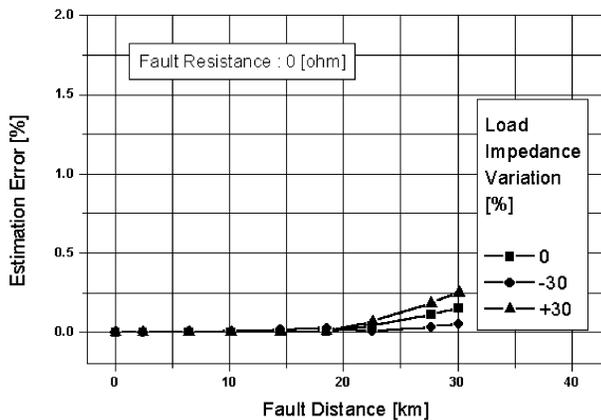
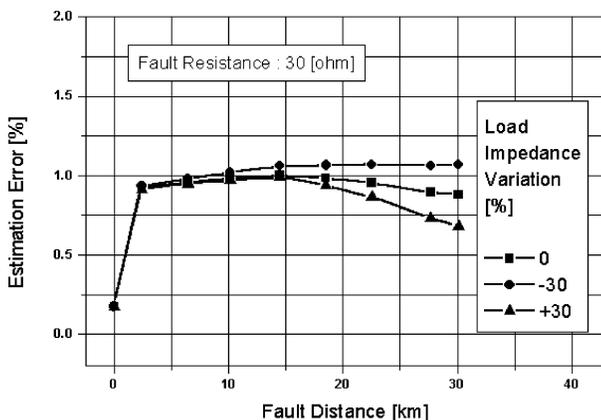


Fig. 17. Fault location error for general impedance model.

Fig. 18. Error with impedance variation of 30% ($R_f = 0$).Fig. 19. Error with impedance variation of 30% ($R_f = 30$).

b) *Effect of load variation:* For average 30% load variation, again mostly the error is kept within 0.25%, showing no accuracy drop for the 0- Ω case as can be seen in Fig. 18. However, some accuracy sacrifice is observed although it is very small in the case of 30- Ω fault resistance case, showing a maximum error of 1.3%, about 0.3% more compared to no load uncertainty case (Fig. 19).

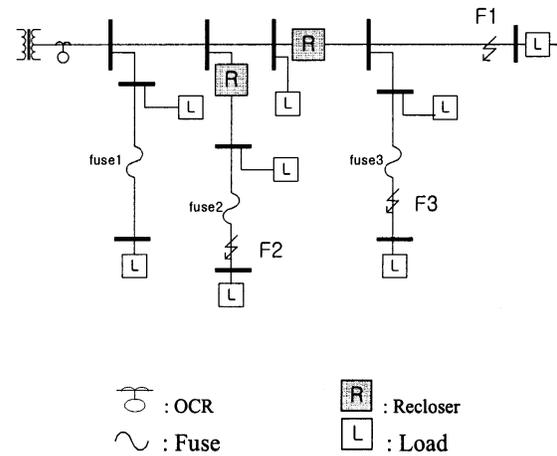


Fig. 20. Example feeder for fault diagnosis.

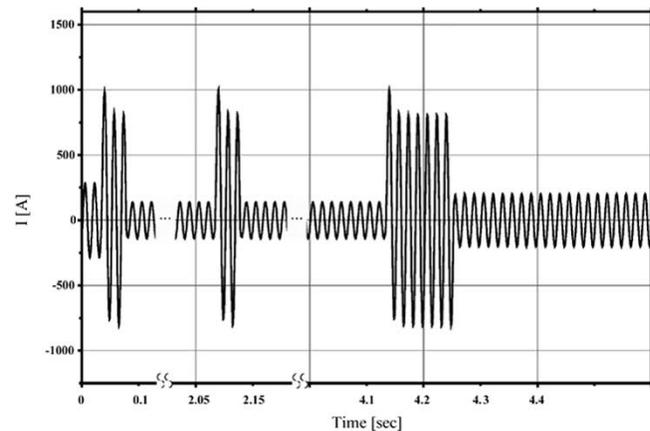


Fig. 21. Fault current waveform.

B. Fault Diagnosis

In order to show the effectiveness of the proposed fault diagnosis scheme, a feeder in Fig. 20 is taken as a test system, which has two reclosers and three fuses. Both reclosers are assumed to have a sequence setting of 2F2D. Simulation for a fault on F2 has been carried out using EMTP. The recorded current is shown in Fig. 21. In the current waveform picture, the real time scale is not used because of the limitation on time axis length to be depicted in the paper. The figure indicates the fault clearing by fuse during recloser delay operation following two fast operations, giving apparent three fast operations and two reclosings.

Suppose the fault location algorithm has yielded two more candidate locations F1 and F3 in addition to the actual fault location F2. Note that the preceding protective device pair is OCR-Recloser for F1, and Recloser-Fuse for both F2 and F3. For each fault location candidate, its expected current waveform pattern derived from the pattern identification rules in Table I is shown in Table IV. According to this table, the device pattern should be OCR-Recloser and, consequently, the first diagnosis step based on the current pattern matching has chosen F2 and F3 as fault location. Note that since both have the same preceding device pair, they cannot be further differentiated using the pattern rules. Now the second step that deals with the load change

TABLE IV
EXPECTED OPERATION FOR EACH FAULT CANDIDATE

Candidate	F1	F2	F3
Protective device	OCR Recloser	Recloser Fuse	Recloser Fuse
Expected operation	Reclosing:3 Fast:2 Delay:2	Reclosing:2 Fast:3	Reclosing:2 Fast:3

TABLE V
EXPECTED LOAD CURRENT

Prefault load current	168.17[A]
load current after fault clearing	120.02[A]
Load below fuse2	46.77 [A]
Load below fuse3	14.37 [A]

analysis before and after the fault clearing is carried out. Fig. 21 shows 168.17-A load current before the fault and 82.70 A after the first and second fast operations, while 120.02 A after the third fast operation, indicating 48.15-A load interruption. With the knowledge on the loading (46.77 A below fuse2) as shown in Table V, the one closer to the interrupted loading is selected, which is F2 in this case.

V. CONCLUSION

This paper proposes an effective fault location algorithm and an intelligent fault diagnosis scheme. The proposed fault location algorithm identifies candidate fault locations using an iterative estimation of load current and fault current at each line section. The diagnosis part determines the actual location by comparing the current waveform pattern with the expected pattern due to operation of the protective devices. If necessary, comparison of the interrupted load with the actual load follows and generates the final decision.

The device that adopts the proposed techniques could be developed into two different kinds depending on whether the distribution automation (DA) is realized or not. In the non-DA system, the proposed technique could be implemented into a digital fault locator to be installed at the substation. It could be a stand-alone device or an additional software function of the digital feeder protection relay. In the DA system, this fault location function would be another application software of the DA central computer. In both cases, the system configuration information and load data need to be provided to the fault locator. Unlike the DA system case, to get the accurate information in the non-DA system might be difficult, especially the loading data. Various simulations changing the load model and loading in addition to the fault location and fault resistance have shown a practically satisfactory accuracy and high robustness to the load variation of the proposed scheme.

REFERENCES

- [1] G. B. Ansell and N. C. Pahalawatththa, "Maximum likelihood estimation of fault location on transmission lines using travelling waves," *IEEE Trans. Power Delivery*, vol. 9, pp. 680–689, Apr. 1994.

- [2] T. Takagi, Y. Yamakoshi, J. Baba, K. Uemura, and T. Sakaguchi, "A new algorithm of an accurate fault location for EHV/UHV transmission lines : Part I – Fourier transform method," *IEEE Trans. Power App. Syst.*, vol. PAS-100, pp. 1316–1323, Mar. 1981.
- [3] Y.-J. Ahn, M.-S. Choi, S.-H. Kang, and S.-J. Lee, "An accurate fault location algorithm for double-circuit transmission systems," in *Proc. IEEE Power Eng. Soc. Summer Meeting*, vol. 3, 2000, pp. 1344–1349.
- [4] A. A. Girgis, C. M. Fallon, and D. L. Lubkeman, "A fault location technique for rural distribution feeders," *IEEE Trans. Ind. Applicat.*, vol. 29, pp. 1170–1175, Nov./Dec. 1993.
- [5] M. E. Hami, L. L. Lai, D. J. Daruvala, and A. T. Johns, "A new traveling-wave based scheme for fault detection on overhead power distribution feeders," *IEEE Trans. Power Delivery*, vol. 7, pp. 1825–1833, Oct. 1992.
- [6] R. Das, M. S. Sachdev, and T. S. Sidhu, "A fault locator for radial sub-transmission and distribution lines," in *Proc. IEEE Power Eng. Soc. Summer Meeting*, vol. 1, 2000, pp. 443–448.
- [7] J. Zhu, D. L. Lubkeman, and A. A. Girgis, "Automated fault location and diagnosis on electric power distribution feeders," *IEEE Trans. Power Delivery*, vol. 12, pp. 801–809, Apr. 1997.
- [8] P. Jarventausta, P. Verho, and J. Partanen, "Using fuzzy sets to model the uncertainty in the fault location process of distribution networks," *IEEE Trans. Power Delivery*, vol. 9, pp. 954–960, Apr. 1994.
- [9] C. A. Reineri and C. Alvarez, "Load research for fault location in distribution feeders," *Proc. Inst. Elect. Eng., Gen. Transm. Dist.*, vol. 146, no. 2, pp. 115–120, Mar. 1999.
- [10] P. Kundur, *Power System Stability and Control*. New York: McGraw-Hill, 1994, pp. 271–275.



Seung-Jae Lee (S'78–M'88) received the B.S. and M.S. degrees from Seoul National University, Seoul, Korea, in 1979 and 1981, respectively, and the Ph.D. degree from the University of Washington, Seattle, in 1988.

Currently, he is a Professor with the Department of Electrical Engineering at Myongji University, Yongin, Korea, where he has been since 1988. He is also Director of the Next-Generation Power Technology Center. His main research areas are protective relaying, distribution automation, and AI

applications to power systems.



Myeon-Song Choi (M'96) received the B.S., M.S., and Ph.D. degrees from Seoul National University, Seoul, Korea in 1989, 1991, and 1996, respectively.

Currently, he is an Associate Professor at Myongji University, Yongin, Korea. He was a Visiting Fellow at Pennsylvania State University, State College, in 1995. His research interests include power system control and protection.

Sang-Hee Kang (S'90–M'93) received the B.S., M.S., and Ph.D. degrees from Seoul National University, Seoul, Korea, in 1985, 1987, and 1993, respectively.

Currently, he is an Associate Professor at Myongji University, Yongin, Korea. He was a Visiting Fellow and a Visiting Scholar at the University of Bath, Bath, U.K., in 1991 and 1999, respectively. His research interests include the development of digital protection systems for power systems using signal processing techniques.

Bo-Gun Jin received the B.S. and M.S. degrees from Myongji University, Yongin, Korea, in 2000 and 2002, respectively. He is currently pursuing the Ph.D. degree at Myongji University.

His main research area is power system control and protection.

Duck-Su Lee received the B.S. and M.S. degrees from Myongji University, Yongin, Korea, in 2000 and 2002, respectively.

In 2002, he joined P&C Technologies Co., Anyang, Korea, where he works on protective relaying.

Bok-Shin Ahn (M'96) received the Ph.D. degree in electrical engineering from Seoul National University, Seoul, Korea.

Currently, he is President and CEO of P&C Technologies Co., Anyang, Korea. He was the head of the Power Systems Department at the Korea Electrotechnology Research Institute (KERI), R&D Center, LG Industrial Systems Co., Anyang, Korea.

Dr. Ahn is a Life-Member of Korean Institute of Electrical Engineers.

Nam-Seon Yoon received the B.S. degree in electrical engineering from Seoul National University, Seoul, Korea.

Currently, he is Head of the R&D Center at P&C Technologies Co., Anyang, Korea. He was Manager and Senior Research Engineer in the Power Systems Department, R&D Center, with LG Industrial Systems Co., Changwon, Korea.

Ho-Yong Kim received the B.S. degree in electrical engineering from Seoul National University, Seoul, Korea, in 1979, and the M.S. and Ph.D. degrees in electrical engineering from the University of Texas at Austin in 1983 and 1985, respectively.

Since 1986, he has been a member of the Korea Electrotechnology Research Institute (KERI), where he is now a Fellow of Power System Research Center of KERI. His research area is R&D of power systems.

Sang-Bong Wee (S'78–M'88), received the B.S., M.S., and Ph.D. degrees from Seoul National University, Seoul, Korea, in 1979, 1981, and 1990, respectively.

Currently, he is an Associate Professor at Korea University of Technology and Education. His main research interest is electrical railroad.