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A Maximum Power Loading Factor (MPLF) Control Strategy for Distributed Secondary Frequency Regulation of Islanded Microgrid

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***Abstract*—Microgrids rely on both primary and secondary frequency control techniques to maintain system stability. Secondary frequency control effectively minimizes frequency fluctuations by adjusting the active power reference in each power inverter, but requires complex and costly inter-equipment communication. In this paper, we propose a distributed secondary frequency control strategy for microgrids containing multiple virtual synchronous generator (VSG) units based on a new maximum power loading factor (MPLF) concept. The MPLF algorithm facilitates power sharing by dynamically identifying the maximum VSG loading factor at each time instance, and then using this value as a unified reference signal for all the VSGs in the microgrid. The active power reference for each VSG will be adjusted based on the unified reference signal, subsequently the secondary frequency control can be realized. The proposed strategy does not require high bandwidth communication since the MPLF data is transmitted among the VSGs using low-bandwidth communication. We also develop small signal models for the control architecture to analyze the influence of major PI control parameters and communication latency. The MPLF control strategy is implemented using custom digital signal processor (DSP) controllers, and experimentally validated using hardware in loop simulations. Finally, the new control paradigm demonstrates significant tolerance for communication delay or failure which we purposely introduced in our investigation.**

***Index Terms*—Virtual synchronous generator, secondary frequency control, power sharing, maximum power loading factor, low bandwidth communication.**

I. Introduction

Microgrids (MGs) greatly promote the utilization of renewable energy. They rely on both primary and secondary frequency control (SFC) to maintain system stability. Secondary frequency control is crucial for reducing the steady-state error of the system frequency and guaranteeing a high supply power quality [1–4]. Therefore, research on SFC for islanded MGs is a key topic nowadays, and so far, significant effort has been devoted to this field. Current SFC strategies for islanded MGs can be divided into two classes: strategies without communication [5-8] and those with communication [9-19].

SFC schemes without communication are mainly of two types: inertial filter-based strategies, which roughly accomplish proportional power sharing [5–7]; the second type utilizes a control mode switch to achieve SFC, combining the advantages of an inertial filter and integral [8]. However, designing parameters for inertial filter-based strategies is complex. To improve proportional power sharing, it is also necessary to extend the delay time of the inertial filter to reduce the effect of local parameters. This causes a negative impact on the system response speed. Further, switch detection highly depends on the switches. Thus, a failure in the switches can worsen the system performance and even lead to oscillations [8]. Additionally, local controllers of the aforementioned non-communication-based SFC strategies must own high computing capabilities in order to provide proportional power sharing in terms of calculation speed and accuracy of the control unit.

The SFC schemes with communication are of two types: centralized control and distributed control. The centralized approach can achieve accurate SFC and power sharing [2], [9], [10]. However, apart from the required high-bandwidth communication system, the approach also highly depends on the central control unit, thereby decreasing the reliability and redundancy of the system. Once the central control unit fails, the SFC of the entire system experiences a direct breakdown. In order to reduce the dependence on the central control unit and communication system, distributed SFC (DSFC) [11–17] was presented. It includes average-algorithm-based DSFC [11–13] and consensus-algorithm-based DSFC [14–19].

The average-algorithm-based DSFC proposed in [11], obtains and averages the complete information in involved distributed generations (DGs). Its reliability is higher than that of the centralized control due to the absent central control unit. However, it has a large quantity of communication data and needs a high and demanding communication bandwidth. In addition, achieving power sharing is difficult because the method uses the average frequency as feedback, ignoring the differences in capacity and control parameters between individual inverters. Though subsequent investigations [12], [13] improved and promoted the method in [11], it has difficulty satisfying the requirements of high communication and reasonable power allocation.

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The consensus-algorithm-based DSFC utilizes the communication between adjacent DG units to achieve the target. This method alleviates the problems regarding high communication requirements and proportional power sharing to a certain degree [14–19]. In [14], a DSFC method with linear input and output feedback was proposed. Its communication between adjacent DG units is simple, whereas power sharing is less considered. In [15], a new method was developed by introducing consistent frequency control. It achieves frequency restoration and accurate active-power allocation. In [16], the consensus control and local proportional–integral (PI) compensation are combined to solve the problems of SFC and active-power sharing in high-R/X MGs. In [17], a consensus control algorithm was proposed, which not only solves the problem regarding SFC and active-power sharing but also that of reactive-power sharing with unknown MG topologies.

Though the consensus-algorithm-based DSFC is already promising, it still has some common limitations that need to be solved:

a) Though the consensus algorithm is achieved via information interaction between adjacent DGs and can reduce the complexity of communication systems, it is coupled with the inverter controllers. Any fault in the inverters directly splits the entire communication system into two parts, thereby affecting the overall coordination. To improve system reliability, the communication line density must be increased, thereby further increasing the complexity and costs of the physical communication layer.

b) Most existing consensus algorithms adopt the idea of an average consistency. Thus, it is still necessary to collect information of multiple DGs, and a high local communication bandwidth is still required.

c) Once the communication is completely disabled, the existing DSFC strategies lose their SFC abilities.

To address the above-mentioned problems, this paper presents a new DSFC strategy for islanded MGs, containing multiple virtual synchronous generators (VSG) with low-bandwidth communication, based on the maximum power loading factor (DSFC-MPLF). The main contributions of the DSFC–MPLF strategy are: a) The concept of MPLF is defined first, thus avoiding diffusing information comparisons between adjacent units or complete MGs. In addition, a differential delay method (DDM) is proposed to select the MPLF automatically, which contributes high reliability and a faster response speed to the system. b) An internal PI frequency compensation loop is added to help each DG unit receive the MPLF from the communication bus directly. This ensures an accurate SFC and proportional power sharing. c) Ultra-low-bandwidth communication can be achieved for the communication bus, which only needs to carry the MPLF data and thereby greatly reduces the communication load. d) The SFC function and stability of the system are less affected by communication latency or failure, which makes the method suitable for situations requiring high-quality frequencies.

The rest of this paper is organized as followings. The principle of DSFC-MPLF and the automatic selection method of MPLF are carefully discussed in Section II. System stability analysis and control parameters optimization is analyzed in Section III. Experimental verifications are presented in Section IV. Finally, Section V concludes this paper.

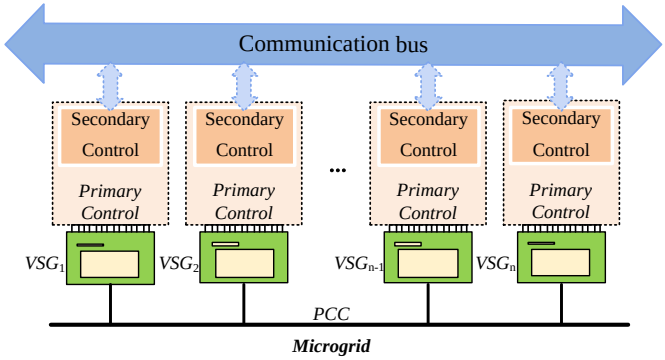

Fig. 1. Structure of VSG-dominated MG with communication functions.

II. DSFC-MPLF Control Strategy

A. Principle of the Proposed DSFC-MPLF

The structure of an MG containing multiple VSGs with communication is shown in Fig. 1. The distributed VSGs exchange information with each other through the communication bus. Primary control can be achieved automatically through virtual inertia and droop characteristics. In order to further eliminate the steady-state frequency error caused by power fluctuations, a new DSFC–MPLF strategy with low-bandwidth communication for MGs containing multiple VSGs is presented. Its basic principle is depicted in Fig. 2.

In Fig. 2, i_{VSGi} is the VSG output current (here i=1,2,…n, n is the number of VSG unit), ΔP_i the VSG active-power compensation, $\dot{\theta}^*_{MG}$ the MG angular frequency reference (f^*_{MG} is the MG frequency reference), $\dot{\theta}_i$ the practical frequency of VSG$_i$, F_{pi} is the local loading factor, F_{pmax} the maximum power loading factor value in the MG, and P_{ei} and P_{ni} are the local practical output power and rated power, respectively.

As shown in Fig. 2, the proposed DSFC–MPLF system consists of three parts: the communication module (1st part), distributed VSG SFC module (2nd part), and primary control module (3rd part). The 1st part is mainly responsible for transmitting the unified reference signal in the MG. The 2nd part receives the reference signal to perform the SFC of the local VSG and power sharing of the complete MG. The 3rd part does the primary control. The core of the DSFC–MPLF strategy

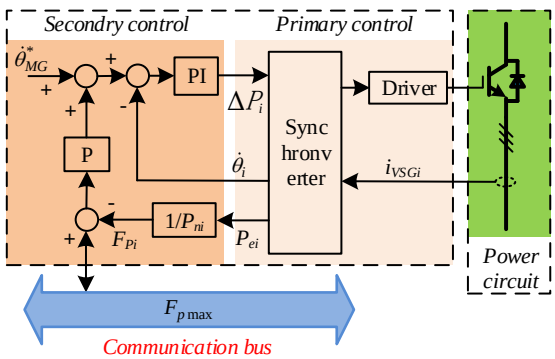

Fig. 2. Scheme of proposed DSFC-MPLF strategy with low-bandwidth communication.

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mostly includes: utilizing the algorithm analyzed in section B to automatically select the VSG with maximum active power loading factor as unified reference value in the MG, then sending its information to other VSGs via the communication module. The local SFC module receives this signal and sets it as reference for the external proportional-control loop. Finally, the inner PI algorithm generates active-power compensation for the primary control module and eventually achieves non-error tracking of the rated frequency.

In order to achieve SFC, power sharing, and simultaneously reduce the communication complexity, a concept using the output loading factor F_p is proposed.

$$F_p = \frac{P_e}{P_n} \tag{1}$$

where, P_e is the VSG active output power, and P_n the rated VSG active power. As shown in Eq. (1), the output loading factor F_p contains rated power and practical output power. Thus, proportional power sharing in the MG can be achieved with a consistent F_p in each VSG unit.

The division achieves that the MPLF is approximately equal to the per-unit value (generally, approximately 0–2), which greatly reduces the bit width requirements of data transmission in communication systems. In addition, the communication bus only needs to transmit the MPLF (defined as F_{pmax} in Eq. (2)), which greatly reduces the data amount as well. Thus, low-bandwidth communication can be achieved.

$$F_{pmax} = max(F_{p1}, F_{p2}, \ldots, F_{pn}) \tag{2}$$

where F_{pmax} is the current value of MPLF in MG.

To further illustrate the principle of the proposed strategy, a detailed diagram of the SFC module in Fig. 2 is presented in Fig. 3. Here, k_{pp} and k_{ip} are the proportional coefficient and integral coefficient of the inner PI part respectively, and k_{pf} is the proportional coefficient of the external proportional control loop. According to Fig. 3, Eq. (3) and (4) can be obtained as follows:

$$\dot{\theta}_{ref} = 2\pi f^*_{MG} + k_{pf}(F_{P\max} - F_{Pi}) \tag{3}$$

$$\Delta P_i = k_{pp}(\dot{\theta}_{iref} - \dot{\theta}_i) + k_{ip}\int(\dot{\theta}_{iref} - \dot{\theta}_i)dt \tag{4}$$

where $\dot{\theta}_i$, $\dot{\theta}_{iref}$ are the practical angular frequency and its reference respectively.

According to Figs. 2 and 3 and Eqs. (1)–(4), the implementation procedure of the proposed DSFC-MPLF can be described as follows:

First, each VSG unit measures the local output power in every sample time and uses Eq. (1) to obtain the local output loading factor F_{pi}.

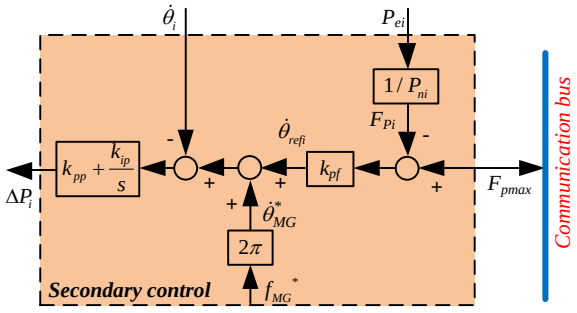

Fig. 3. Detailed control diagram of the SFC module in a VSG unit.

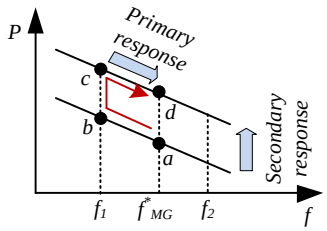

Fig. 4. Frequency control process of DSFC-MPLF.

Second, F_{pi} and F_{pmax} obtained from the communication bus are inserted into Eq. (3) to obtain the angular frequency reference $\dot{\theta}_{iref}$ for the microgrid.

Third, the error between angular frequency reference and the practical value $\dot{\theta}_i$ is inserted in Eq. (4) to obtain the active power reference compensation.

Finally, the local VSG active power can be adjusted according to the compensating requirements, and SFC can be realized simultaneously.

In order to explain why the secondary frequency regulation and power sharing can be realized with the above process finished. The situation when system is stable is introduced in detail:

When the system is stable, $F_{pmax} = F_{pi}$ occur in the MPLF VSG unit. At this time instant, the output of the external proportional-control loop is zero, and the DSFC–MPLF is degraded to local frequency tracking with the fixed rated frequency f^*_{MG}. Moreover, owing to the inner PI loop, the local frequency is always consistent with the rated frequency of the system, i.e., non-error tracking can be realized.

The additional frequency control mechanism of implementation procedure above was shown in Fig. 4. Primary frequency control can be regarded as a lateral movement along the curve, whereas SFC can be treated as a vertical transition of the curve. Assuming that the initial state of the system is running at the rated point ***a***. When the loads increase, the system frequency decreases. Thus, the operating point shifts from point ***a*** to ***b***. At this time instant, the inner SFC loop in the secondary-control module quickly generates active-power compensation in accordance with the frequency error, and sends it to the primary-control module, thereby shifting the operating point from point ***b*** to ***c***. Finally, under primary control, the operating point gradually moves to point ***d***, i.e., frequency restoration is achieved. During the regulation process, the communication system responses for transmitting the reference signals to adjust the rated frequency of non-F_{pmax} VSG units and to complete the power distribution in the MG. Hence, SFC and proportional power sharing can be achieved.

Actually, the communication failure is an inevitable problem. For the proposed DSFC-MPLF, F_{pi} of the local VSG$_i$ replaces F_{pmax} automatically, which causes the external proportional-control loop output to equal zero. The following process is the same as in the aforementioned stable situation, that is, non-error of frequency tracking can be continued.

B. Automatic Selection Method of MPLF

The basic principle and implementation process of the proposed DSFC–MPLF method are explained in Section II-A. However, the automatic selection of the VSG unit with F_{pmax} is

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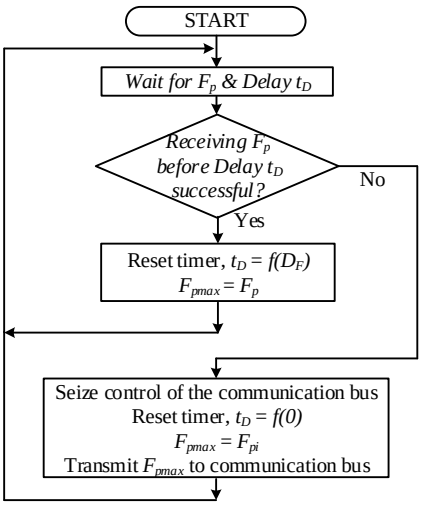

Fig. 5. Specific flow chart of the proposed differential delay method.

a key technical issue in practical applications—particularly, regarding the VSG unit self-judgment and the communication bus control right transfer.

To solve this problem, a DDM is proposed in this section. It uses the controller area network (CAN) communication bus as physical basis (i.e., each VSG communication interface is unified as CAN bus protocol in the MG), and refers to the communication principle in the consensus algorithm. Fig. 5 presents a specific flow chart of the method, where F_p is the received power loading factor, F_{pi} the local VSG power loading factor, F_{pmax} the value of the present reference in the MG, and D_F and t_D are defined as follows:

$$D_F = F_{pi} - F_{p\max} \tag{5}$$

$$t_D = f(D_F) \tag{6}$$

where D_F is the error between F_{pi} and F_{pmax}, t_D is the differential delay time. Considering that the maximum output power of inverter is usually twice the rated value, the maximum value of D_F is 4.

It is assumed that Eq. (6) can be depicted by three typical functions *a*, *b*, and *c*, as shown in Fig. 6.

When Eq. (6) is a convex function like curve *a* in Fig. 6, the larger the relative output power of the VSG unit is, the larger and smaller are D_F and t_D, respectively. Moreover, the closer D_F is to D_{Fmax}, the larger and greater are the slope of the curve and sensitivity, respectively. However, this function type is less sensitive for small D_F values. When choosing a concave function like curve *c* in Fig. 6, the larger the VSG output power is, the larger is D_F. However, when D_F is closer to D_{Fmax}, the smaller the slope of the curve is, the lower is the sensitivity. If a linear function like *b* in Fig. 6 is chosen, the slope is constant,

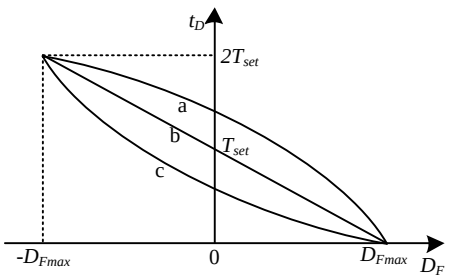

Fig. 6. Three typical t_D-D_F curve.

i.e., the sensitivity of D_F to t_D remains unchanged in the complete interval. Considering the realization simplicity and accurate together, curve *b* is chosen for this study.

The basic idea of the DDM is to calculate the delay time t_D according to the error between the received output loading factor F_p and local output loading factor F_{pi}. Different VSGs own different t_D values and VSGs with larger F_{pi} values have shorter delay times. Consequently, VSGs with larger F_{pi} values have priority to obtain the communication right. I.e., according to Eq. (7), the MPLF unit is automatically regarded as system reference. Thus, it coordinates all VSGs in the MG.

$$t_D = -kD_F + T_{set} \tag{7}$$

The detailed operation steps in Fig. 5 are as follows:

Step 1: The local VSG waits and detects whether there is any output loading factor F_p sent from the communication bus.

Step 2: If the local VSG receives data F_p from the communication bus first, this F_p is the present F_{pmax} in the MG. Hence, at this time, the local F_{pi} does not need to participate in grabbing the communication right. The local delay timer is immediately reset and the new delay time t_D is calculated with Eq. (7) to wait for the next grabbing cycle. The received F_p serves as reference for the external proportional-control loop of the local SFC module. The local active output power reference is then adjusted via the obtained frequency compensation with the inner PI loop.

Step 3: If the local delay time t_D is reached first, F_{pi} is the present F_{pmax} in the MG. The VSG unit acquires the communication right and sends its F_{pi} to other units as the new F_{pmax} in a one-to-many relation. Simultaneously, the local delay timer needs to be reset, and a new delay time $t_D = T_{set}$ is obtained in accordance with Eq. (7). Now, the local VSG waits and prepares itself for grabbing the communication right in the next cycle. At this moment, since $F_{pi} = F_{pmax}$ in this VSG unit, the output of the external proportional-control loop is zero, and the local SFC is degraded with local frequency tracking to the fixed rated frequency f^*_{MG}.

When the system reaches a steady state, D_F of each VSG remains zero and the period time of the system communication is stable for T_{set}.

The proposed methods do not have to specify the priority orders, serial numbers of each unit, or a specific fixed unit in advance. When some VSGs fail or even if the MPLF unit fails, the proposed methods selects the second largest MPLF VSG as the new leader in accordance with the delay time. Here, a new system reference is formed to ensure the reliability in MGs.

III. System Stability Analysis And Control Parameters Optimization

A. Small-signal Analysis and Parameters Optimization of the DSFC-MPLF-based VSG

In order to optimize the parameters in the proposed strategy, a small-signal model of the DSFC–MPLF strategy is analyzed. Because single VSG stability is the foundation of whole system, this model mainly focuses on a single VSG unit and ignores voltage fluctuations in the MG [20]. The stable boundaries and relations between the three introduced parameters k_{ip}, k_{pp}, and k_{pf} are analyzed using the small-signal model.

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Figure 7 shows the VSG topology discussed in [3]. It comprises a power part and an electric control part. The power part shown in Fig. 7(a) includes the DC bus capacitor, inverter, and filter, which are used to convert the DC power into industrial-frequency AC power. Here, L_{sg} and R_{sg} are the equivalent inductance and resistance between the inverter output and circuit breaker (CB), respectively; L_g and R_g are the equivalent inductance and resistance between the CB and point of common coupling (PCC), respectively; i_g is the output current of the inverter; e is the reference voltage, whose magnitude is expressed as E; E_n is the reference voltage and u_{pcc} the PCC voltage; $\dot{\theta}_n$ is the reference frequency; P_n and Q_n are the reference active power and reactive power, respectively (usually equal to the rated active power and reactive power); The core of the electric control part is the virtual synchronized control unit shown in Fig. 7(b); J is the rotational inertia; D_p is the damping factor; K is the reactive-power regulation inertia coefficient; D_q is the voltage drooping coefficient [21], [22].

$$\begin{cases} T_e = M_f i_f < i, \sin\theta > \\ Q = -\dot{\theta} M_f i_f < i, \cos\theta > \\ e = \dot{\theta} M_f i_f \sin\theta \end{cases} \tag{8}$$

Table I lists the first VSG parameters.

The impedance between the VSG and PCC in an MG is usually the resistor inductance. Considering that the filter inductance is X_{sg}>>r [22], the inverter output power can be expressed with Eq. (9), where X_s is the equivalent reactance between VSG and PCC in an MG.

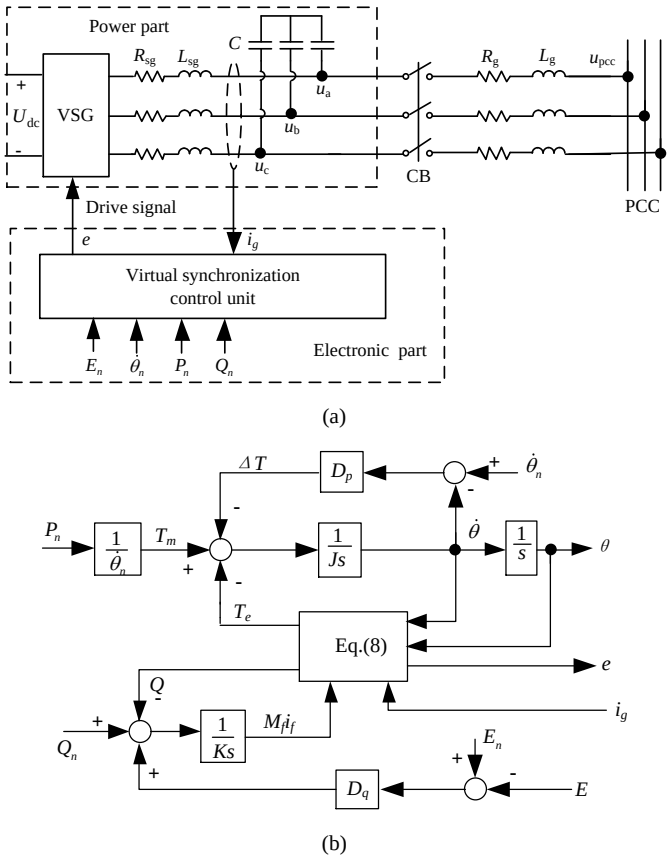

Fig. 7. Schematic of VSG, (a) Power part, (b) Electronic part.

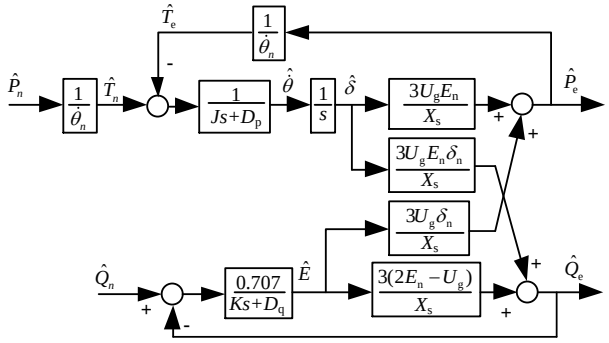

Fig. 8. Small signal model of the VSG within 's' domain.

Tab. I VSG Parameters.

Parameters	Value	Parameters	Value
J	0.5066	$\dot{\theta}_n$ (rad·s^{-1})	2pi·50
K	6283.185	E_n(V)	310
D_p	5.066	k_{pf}	8
D_q	200	k_{pp}	10
P_n(kW)	5	k_{ip}	500
Q_n(kVar)	4		

$$\begin{cases} P_e = \dfrac{3U_{pcc}E}{X_s}\sin\delta \\ Q_e = \dfrac{3(E - U_{pcc}\cos\delta)E}{X_s} \end{cases} \tag{9}$$

The detailed process of small signal modeling of VSG is shown in the appendix. And the result of small signal modeling of VSG is shown in Fig. 8.

According to [23], when X_o<0.1 pu, δ_n<=0.2 rad. In this case, the coupling of active and reactive power is less than 1, which can be approximately regarded as a mutual decoupling. Based on this assumption and the combination of Eqs. (2)–(4) with Fig. 8, the power frequency small-signal model of the DSFC–MPLF-based VSG within the 's' domain is established (Fig. 9).

In Fig. 9, $\hat{F}_{p\max}$ and $\hat{\dot{\theta}}^*_{MG}$ represent small variations of the MPLF and frequency reference in the MG, respectively; $\hat{P}_{QE}$ in Eq. (14) represents the coupling between P and Q; $H(s)$ in Eq. (15) stands for the filter function, which contains the delay effect of the main circuit output filter and sampling filter.

$$\hat{P}_{QE} = \frac{3U_{pcc}\delta_n\hat{E}}{X_s} \tag{10}$$

$$H(s) = \frac{1}{T_1 s + 1} \tag{11}$$

where δ_n and $\hat{E}$ are the variations of the rated power angle and the internal voltage in a VSG, respectively; T_1 is the inertia time constant.

F_{pmax} is obtained by the low-speed communication system. Hence, its speed changes are slower than those of the internal PI control loop. Since the actual MG frequency is usually a constant, the per-unit of line impedance is usually below 0.1 pu.

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By neglecting the effects of the MG voltage and filter resistor, it can be deduced that the coupling of the reactive and active power is well below 1 (decoupled) [20]. Based on the aforementioned approximation and equivalence analysis, the small-signal closed-loop transfer function $TF1(s)$ of P_{ni} and P_{ei} can be derived as Eqs. (12)–(14), where P_{ni} and P_{ei} are the active-power reference and its practical value in the DSFC–MPLF -based VSG.

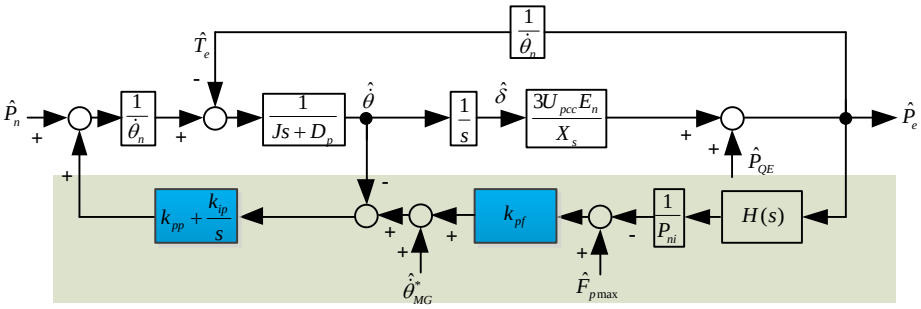

Fig. 9. Small signal model of DSFC-MPLF-based VSG within 's' domain.

$$TF1(s)=\frac{P_{ei}}{P_{ni}}=\frac{b_0s^2+b_1s+b_2}{a_0s^4+a_1s^3+a_2s^2+a_3s+a_4} \tag{12}$$

where,

$$\begin{cases} b_0=9U_{pcc}^2E_n^2P_nT_1 \\ b_1=9U_{pcc}^2E_n^2P_n \\ b_2=0 \end{cases} \tag{13}$$

$$\begin{cases} a_0=3U_{pcc}E_nP_n\dot{\theta}_nZ_sJT_1 \\ a_1=3U_{pcc}E_nP_n\dot{\theta}_nZ_s(D_pT_1+J)+3U_{pcc}E_nP_nZ_sk_{pp}T_1 \\ a_2=3U_{pcc}E_nP_n(3U_{pcc}E_nT_1+\dot{\theta}_nZ_sD_p)+ \\ \quad 3U_{pcc}E_nP_nZ_s(k_{pp}+k_{ip}T_1) \\ a_3=9U_{pcc}^2E_n^2P_n+3U_{pcc}E_n(3U_{pcc}E_nk_{pf}k_{pp}+Z_sP_nk_{ip}) \\ a_4=9U_{pcc}^2E_n^2k_{pf}k_{ip} \end{cases} \tag{14}$$

Based on the topology in Fig. 1, the impact of parameters k_{pf}, k_{ip}, and k_{pp} on the stability are analyzed to provide better designed parameters for the system. The VSG parameters are shown in Tab. I and Tab. II in Section IV and are used for $TF1(s)$. Figure 10 shows the pole-zero distributions of Eq. (12) when k_{pf}, k_{ip}, and k_{pp} vary, i.e., k_{pf} varies from 0 to 25, k_{ip} from 0 to 10000, and k_{pp} from 0 to 600.

As shown in Fig. 10, the improved VSG function has four poles, which are located on the left side of the imaginary axis when the three parameters are small. The system is stable at the beginning. However, when any parameter of k_{pf}, k_{ip}, and k_{pp} increases, the other two poles cross the imaginary axis, thereby resulting in system instabilities. Particularly, when k_{pf} increases to 12.4, k_{ip} to 7961.5, or k_{pp} to 297.6, the improved VSG becomes unstable.

To analyze the relations between k_{pf}, k_{ip}, and k_{pp}, Fig. 11 depicts the 3D stabilization interval of the improved VSG, where the x-, y-, and z-axes represent k_{ip}, k_{pp}, and k_{pf}, respectively. According to Fig. 11, k_{pf} increases continuously with constant k_{ip} and k_{pp}. When any of the system poles is moved to the right side of the imaginary axis, the k_{pf} value is noted down and the point is marked in the 3D coordinate system. The values of k_{ip} and k_{pp} are changed until stable and unstable boundaries are obtained. Equation (15) represents the mathematical description of the stable region with S as the surface between stable and unstable region.

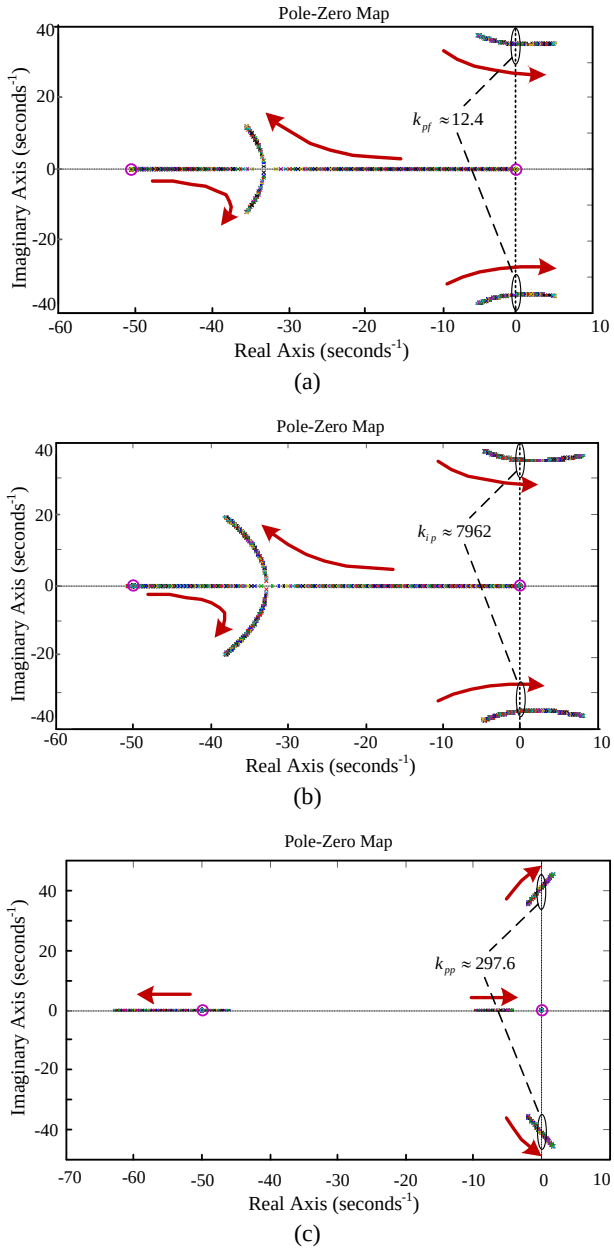

Fig. 10. System Pole-Zero distributions of the DSFC-MPLF-based VSG, (a) k_{ip} = 5000, k_{pp} =10, k_{pf} varies, (b) k_{pf} = 8, k_{pp} = 10, k_{ip} varies, (c) k_{ip} = 5000, k_{pf} = 10, k_{pp} varies.

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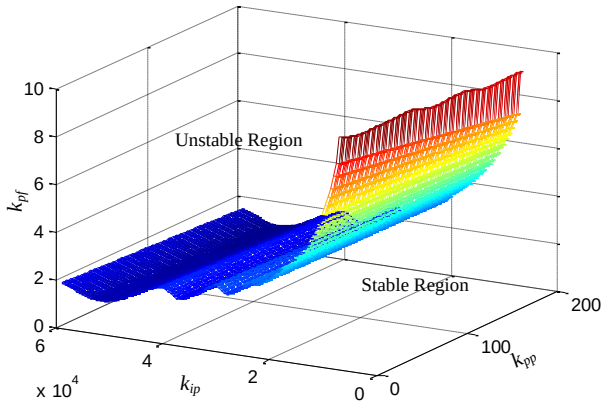

Fig. 11. Stability regions of parameters k_{pf}, k_{ip} and k_{pp} in the proposed DSFC-MPLF.

$$\begin{cases} S(k_{ip}, k_{pp}, k_{pf}) > 0 \\ k_{ip} > 0, k_{pp} > 0, k_{pf} > 0 \end{cases} \tag{15}$$

As shown in Fig. 11, the stable area is located on the right side between the x–y plane and the depicted camber surface. In addition, with increasing k_{pf}, k_{ip}, and k_{pp}, the stability region of the system decreases. When one of the three parameters increases, the margin of the stable regions of the others decreases. More attention should be paid to this behavior for practical application designs.

The above small-signal analysis is based on a single VSG with the proposed method. The outcome is a prerequisite to ensure the stable operation of a single VSG in actual applications. However, it must be noted that stability of a single VSG may not guarantee that of the entire system, and the stability region shown in Fig. 11 is a sub- region of the entire system due to the nonlinear characteristics.

B. Effect of communication delay, data loss, and communication failure on DSFC-MPLF

1) Effect of communication delay, data loss, and communication failure on differential delay method

For the CAN bus protocol, only one device can occupy the communication bus at the same time. So, when a VSG is sending data, the other VSGs will not be able to repeat this action. Otherwise this communication will fail due to the data conflict. The operation process of the DDM with communication delay is shown in Fig. 12. VSG_1 is assumed to have the maximum loading factor unit in the previous cycle.

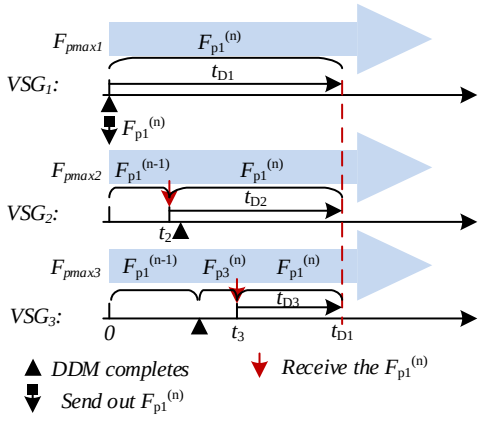

Fig. 12. Operation process of DDM in one cycle when there is communication delay.

In Fig. 12, $F_p^{(n-1)}$ represents loading factor in the previous cycle, $F_p^{(n)}$ represents the current cycle one; F_{pmax1}, F_{pmax2} and F_{pmax3} are the actual loading factor references of three VSGs; t_2 and t_3 are the total communication delay from VSG_1 to VSG_2 and VSG_3, respectively (including delay in the communication bus, equipment, and the DSP controller); t_{D1}、t_{D2} and t_{D3} are the differential delay which are defined in Eq. (6) in the current cycle of three VSGs, respectively.

Assuming that VSG_1 has the largest loading factor in the previous cycle, then it will be the first one to complete the differential delay according to Eq. (5) and Eq. (7). Then as shown in Fig.12, it will occupy the communication bus to broadcast its own loading factor, $F_{p1}^{(n)}$, at $t = 0$. The situation of VSG_2 and VSG_3 are analyzed in the following subsections.

Analysis I: Effect of communication delay, data loss, and communication failure on automatic selection of MPLF-unit.

After VSG_1 completes the previous differential delay, it immediately occupies the communication bus and restarts the current differential delay (t_{D1}) before sending data to VSG_2 and VSG_3. During the period of t_{D1}, the controller will forbid the data-sending request from VSG_2 and VSG_3 to the bus.

When VSG_2 receives the data successful before the end of t_{D1}, VSG_2 will first cancel the request to send itself data, and will set F_p as the reference F_{pmax}. The differential delay t_{D2} can then be started. If VSG_2 wants to occupy the communication bus and become the system leader for the next period, Eq. (16) must be satisfied.

$$t_2 + t_{D2} < t_{D1} \tag{16}$$

Similarly, after VSG_2 becomes the system leader, if VSG_1 wants to regain the communication right from VSG_2, Eq. (17) must be satisfied by assuming that the time-delays of data sending between VSG_1 and VSG_2 are equal.

$$t_2 + t_{D1} < t_{D2} \tag{17}$$

Therefore, even when there is a communication delay, the MPLF-VSG can still effectively send signals to other VSGs. The main influence is that VSGs with larger communication delay are harder to obtain the communication right than those with no delay as shown in Eq. (16). Nonetheless, once a VSG becomes the system leader, the above situation will be reversed as shown in Eq. (17). So, certain communication delay grants the MPLF-VSG with a hysteresis nature, which can prevent the frequent changes of leadership unit and is beneficial to the system stability.

On the other hand, if there is data loss, e.g. if VSG_2 fails to receive one data from VSG_1 (as shown in Fig.5) before the end of t_{D1}, the controller will not be able to cancel VSG_2's transmission require. And the VSG_2 will automatically send its own loading factor to the others once it completes the differential delay. This case is equivalent to adding another differential delay process in the communication rights competition. Each VSG will reset the differential delay time according to the received data to re-choose a new MPLF-unit. Thus, data loss can hardly affect the selection of the system MPLF-unit.

The final situation is the failure of communication between VSGs, which is different from the normal data-delay. In this case, the communication failed-VSG cannot detect the occupancy of the CAN bus, thus it is unable to receive the F_p sent by the others and will automatically consider itself to be

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the MPLF-unit. During this period, the failed-VSG can only finish the SFC and no longer has the power sharing capability.

When analysis of automatic selection of MPLF unit is completed, variations of reference signal inside each VSG should be analyzed next.

Analysis II: Effect of communication delay, data Loss, and communication failure on the reference signal F_{pmax} of each VSG

It can be seen from Fig. 12 that VSG_1 immediately occupies the communication bus and restarts the next differential delay after it completes the differential delay. At this time, the reference signal $F_{\mathrm{pmax1}} = F_{\mathrm{p1}}^{(\mathrm{n})}$ and will maintain until the start of the next cycle.

For VSG_2, it still uses the reference signal $F_{\mathrm{p1}}^{(\mathrm{n-1})}$ of the previous cycle as its own reference before it receives $F_{\mathrm{p1}}^{(\mathrm{n})}$. After it receives the data sent by VSG_1, it will use $F_{\mathrm{p1}}^{(\mathrm{n})}$ as the reference signal until the beginning of the next cycle.

For VSG_3, there are three periods due to receiving $F_{\mathrm{p1}}^{(\mathrm{n})}$ successfully late for DDM completes of the VSG_3. First period is before VSG_3's DDM finish, it regards the reference signal $F_{\mathrm{p1}}^{(\mathrm{n-1})}$ in the previous cycle as its own reference, which is same as that the situation of VSG_2. Second period is between VSG_3 completes its own DDM and the data from VSG_1 arrives VSG_3. The reference signal is updated to VGS_3's own loading fact $F_{\mathrm{p3}}^{(\mathrm{n})}$, although it cannot send this out due to the occupation of CAN by VSG_1. The final period is after receiving data from VSG_1 successful, the VSG_3's reference signal is updated to be $F_{\mathrm{p1}}^{(\mathrm{n})}$.

Through the above analysis, it can be seen that the VSG_i will use its own $F_{\mathrm{p}}^{(\mathrm{n})}$ as a reference when the self-differential delay is completed before the successful communication completion (too long communication delay) or the communication fails. For the too long communication delay, the VSG will keep its own $F_{\mathrm{p}}^{(\mathrm{n})}$ as a reference before successfully receiving the new loading factor from other VSGs. This segment time, i.e., second time period in the previous paragraph, is similar to a "pause state". When the loading factor from other VSGs is received, the VSG will end this pause state and updates the system MPLF as the reference signal. Thus it will participate in the SFC and power sharing.

When the communication data is lost, after the VSG have completed the differential delay, it will maintain the output condition before receiving the loading factor from other VSGs in the next period. And it will be able to continue to participate in the SFC and power sharing as well.

However when the communication fails in one VSG, it will always use its own $F_{\mathrm{p}}^{(\mathrm{n})}$ as the reference signal since it cannot receive data from others. This situation is different from the previous delay situation in VSG_3. Under this condition, the communication failed-VSG only has the SFC capability but no power sharing.

Generally, the CAN-bus-based DDM can ensure that the system only has one unified reference signal in the condition of communication delay or data loss, which can guarantee the SFC and power sharing characteristics. Even in the condition of communication failure, it can still guarantee the system SFC capability.

2) Effect of communication delay, data loss, and communication failure on the stability of the parallel VSG supply system

According to the analysis in the previous section, there is only one unified reference signal in the whole system even under the condition of communication delay or data loss. This section will further analyze the effects on the stability of the parallel VSG supply system.

Assuming that VSG_1 is the current system leader, VSG_2 and VSG_3 use F_{p1} as the reference. The communication delays of F_{p1} to VSG_2 and VSG_3 are t_2 and t_3, respectively, as described by $G_{\mathrm{d2}}(\mathrm{s})$ and $G_{\mathrm{d3}}(\mathrm{s})$ in Eq. (18), Eq. (19).

$$G_{d2}(s) = \frac{1}{1+t_2 s} \tag{18}$$

$$G_{d3}(s) = \frac{1}{1+t_3 s} \tag{19}$$

The system model with considerations of communication delay is shown in Fig. 13.

In Fig. 13, $G_{i1}(\mathrm{s})$-$G_{i3}(\mathrm{s})$ are expressions of the inner control blocks (i = 1, 2, 3); $G_{\mathrm{Fp}}(\mathrm{s})$ represents the filter when calculating loading factors. By combining with Fig. 9, the following equations can be deduced.

$$G_{i1}(s) = \frac{3U_{pcc}E_{ni}}{s(J_i s + D_{pi})X_{si}\dot{\theta}_n + 3U_{pcc}E_{ni}} \tag{20}$$

$$G_{i2}(s) = H(s)\cdot\frac{1}{P_{ni}} \tag{21}$$

$$G_{i3}(s) = k_{pfi}\frac{k_{ppi}s + k_{ipi}}{s} \tag{22}$$

$$G_{i4}(s) = \frac{P_{ni}\dot{\theta}_n(J_i s + D_{pi})^2 s X_{si}}{k_{pfi}H(s)} \tag{23}$$

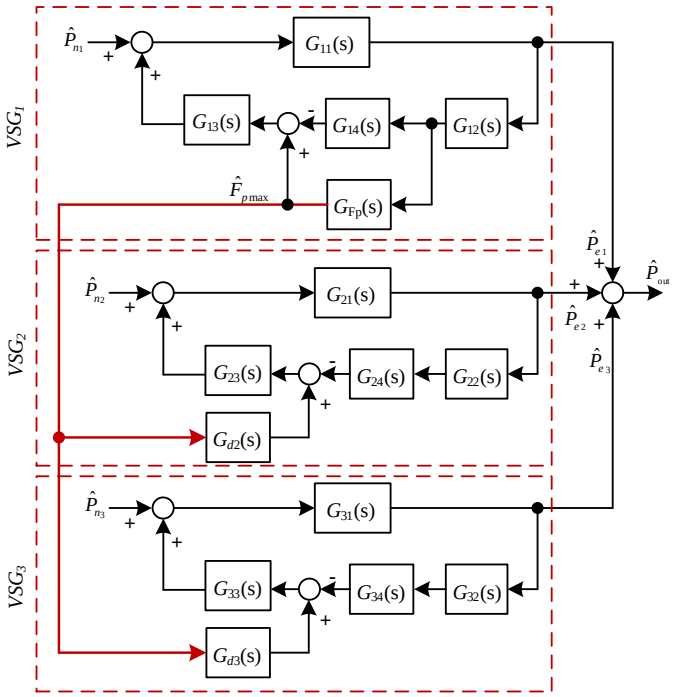

Fig. 13. System model with considerations of communication delay.

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$$G_{Fp}(s)=\frac{1}{1+t_{Fp}s} \tag{24}$$

In order to investigate the effect of the communication on the system stability, VSG_2 and VSG_3, which accommodate communication delays, will be studied in detail by building a closed-loop control model. In this model, F_p is sent from VSG_1 to VSG_2 and VSG_3, and then VSG_2 and VSG_3 will change their own output, which will affect the system's overall output and suppress the change of F_p. The detailed control loop model is derived as follows.

If the active loss in the system is ignored, the load power, P_L, should be as following:

$$P_{e1}+P_{e2}+P_{e3}=P_L \tag{25}$$

By differencing (25), (26) can be derived.

$$\hat{P}_{e1}=\hat{P}_L-\hat{P}_{e2}+\hat{P}_{e3} \tag{26}$$

With reference to Fig. 13, transfer functions of P_{e1} and P_L can be given as (27).

Then, substituting Eq. (11), (20)-(24) into Eq. (27), the system's transfer function can be concluded.

$$TF2(s)=\frac{P_{e1}}{P_L}=\frac{(1+G_{21}G_{23}G_{d2})(1+G_{31}G_{32}G_{34}G_{33})}{(1+G_{21}G_{22}G_{24}G_{23})(1+G_{31}G_{32}G_{34}G_{33})+G_{Fp}G_{12}(G_{21}G_{23}G_{d2}(1+G_{31}G_{32}G_{34}G_{33})+G_{31}G_{33}G_{d3}(1+G_{21}G_{22}G_{24}G_{23}))} \tag{27}$$

Stability of the control system can be analyzed by the pole distribution of TF2(s). The system zero-pole distribution when the communication delay of VSG_2 varies from 0s to 5s is shown in Fig. 14. System parameters are shown in Table I, II and III.

It can be seen from Fig. 14 that when communication delay in VSG_2 increases from 0 to 5s, the poles gradually approaches to the imaginary axis but never across 0, which means that the system is always in a stable state. Considering the limiting case, i.e. when t_2 is infinite, VSG_2 will use its own loading factor as the reference signal based on the previous analysis. And its communication with other VSGs will be cut off. The entire system will no longer be a closed loop as shown in Fig.15. In Fig. 15, $G_{s1}(s)$, $G_{s2}(s)$ and $G_{s3}(3)$ represent the P_n -P_e transfer functions of the three VSGs, respectively. According to the control theory, when two sub-systems are stable respectively, the entire system will be stable. Therefore, even when the delay is infinite, the system will still be in a stable state.

When the communication data is lost, the VSG will hold its output before successfully receiving the loading factor from others. This is similar to the above infinite delay situation, and there will no stability problems due to the loss of closed-loop communication.

When the communication fails, the VSG will use its own loading factor as a reference. This is also similar to the case of the infinite communication delay. The entire system can be decomposed into the two subsystems as shown in Fig. 15. Since there is no closed-loop communications, the entire system will be in a stable state as long as the sys1 and sys2 are stable.

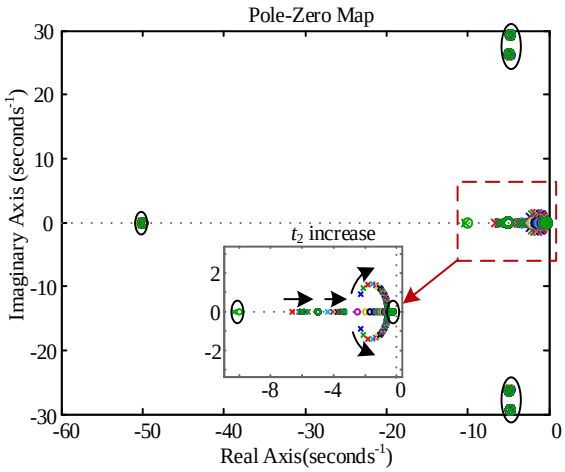

Fig. 14. System Pole-Zero distributions when communication delay of VSG_3 t_3 = 0.1s and communication delay t_2 of VSG_2 varies from 0s to 5s.

To sum up, when there is communication delay or data loss, the proposed method can ensure that the microgrid will always has only one unified reference signal to guarantee the SFC and power sharing; when the communication fails, the SFC function can still be guaranteed.

In addition, the system stability will not be affected regardless of a long communication delay (5s), data loss or even communication failure.

IV. Experimental Verification

To demonstrate the feasibility of the proposed strategy, controller hardware-in-the-loop (CHIL) experiments are carried out. Figure 16 presents the VSG-dominated islanded MG of the experiment. Three VSGs are employed to better verify the power sharing function.

The main circuit is simulated by RT-LAB real-time system (produced by Opal-RT), and the control system consists of three individual digital signal processor (DSP, TMS320F28335). Every VSG is controlled by a DSP. And the CAN bus communication between three DSPs is realized by copper shielded twisted pair lines.

The communication speed is set to 10 kbps, default communication period is T = 0.2 s, differential delay coefficient is k = 0.025, and T_{set} = 0.2 s. The rated frequency, single-phase voltage, active power, and reactive power of the MG are 50 Hz, 220 V, 23 kW, and 13 kVar, respectively. The inverter-switching frequency is 6.4 kHz, the output filter L = 3 mH, and C = 6 uF. The power calculation and loading factor calculation low-pass filter parameter in the DSP program is T_1 = 0.02s, t_{FP} = 0.04 s, respectively. Table II lists the three VSG parameters, and Tab. III presents the SFC parameters.

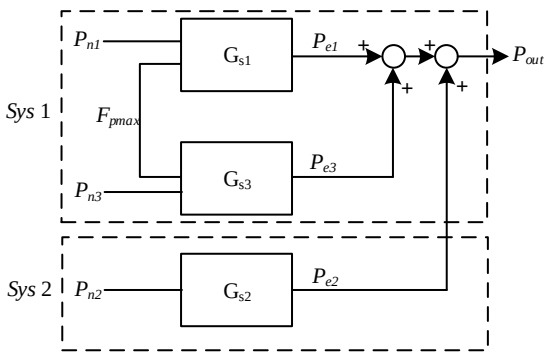

Fig. 15. System equivalent diagram when communication delay in VSG_2 is infinite.

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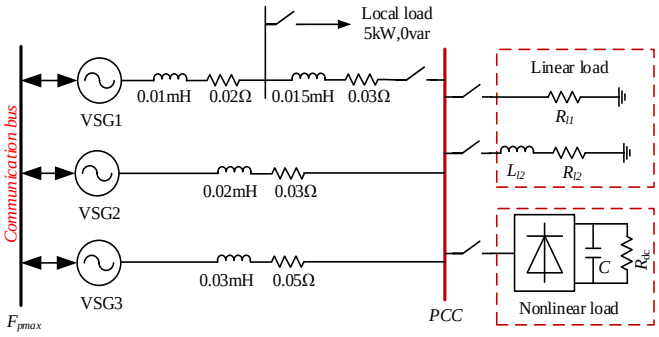

Fig. 16. Experiment topology of VSG controlled islanded MG.

In order to verify the performance of the proposed strategy, this study conducts a set of experiments using different angles. The experiments are explained in detail in the following sections.

Tab. II VSG Parameters.

	VSG_1	VSG_2	VSG_3
J	0.5066	0.8106	1.0132
K	6283.185	9424.778	15707.963
D_p	5.066	8.106	10.132
D_q	200	300	500
P_n(kW)	5	8	10
Q_n(kVar)	4	4	5
$\dot{\theta}_n$ (rad·s^{-1})	2pi·50	2pi·50	2pi·50
E_n(V)	310	310	310

Tab. III P and PI parameters in VSGs

	VSG_1	VSG_2	VSG_3
k_{pf}	8	10	12
k_{pp}	10	15	20
k_{ip}	500	300	200

A. Basic Function Verification of Frequency Restoration and Power Sharing

These experiments indicate the frequency restoration function of the proposed strategy when power fluctuates. Two sets of experiments (Test I, II.) have been designed and carried out. Test I aims to verify the basic functions of the proposed method, and Test II targets at verifying the robust operation of the proposed method under various operating conditions.

In Test I, the specific process is shown as follows: in the initial stage, the VSG controlled MG operates with light load (P = 12kW and Q = 5kVar). At t = 50s, P becomes 30kW. At t = 65s, the DSFC-MPLF is activated. At t = 80s, P becomes 18kW. At t = 95s, P becomes 30kW again. At t = 110s, VSG_1 is cut off for fault.

In Test II, the VSG controlled MG operates with light load (P = 12kW and Q = 0kVar) in the initial stage; at t = 65s, the DSFC-MPLF is activated; at t = 80s, the local load (P = 5kW, Q = 0kVar) is connected; at t = 95s, the low power factor load (P = 1kW and Q = 10kVar) is connected to PCC, and the PCC load power factor decrease from 1.0 to 0.793; at t = 110s, a same low power factor load is connected to PCC, and the PCC load power factor decrease from 0.793 to 0.573; at t = 125s, a nonlinear load (three phase rectifier) about 3kW is connected to PCC; at t = 140s, the nonlinear load is cut off.

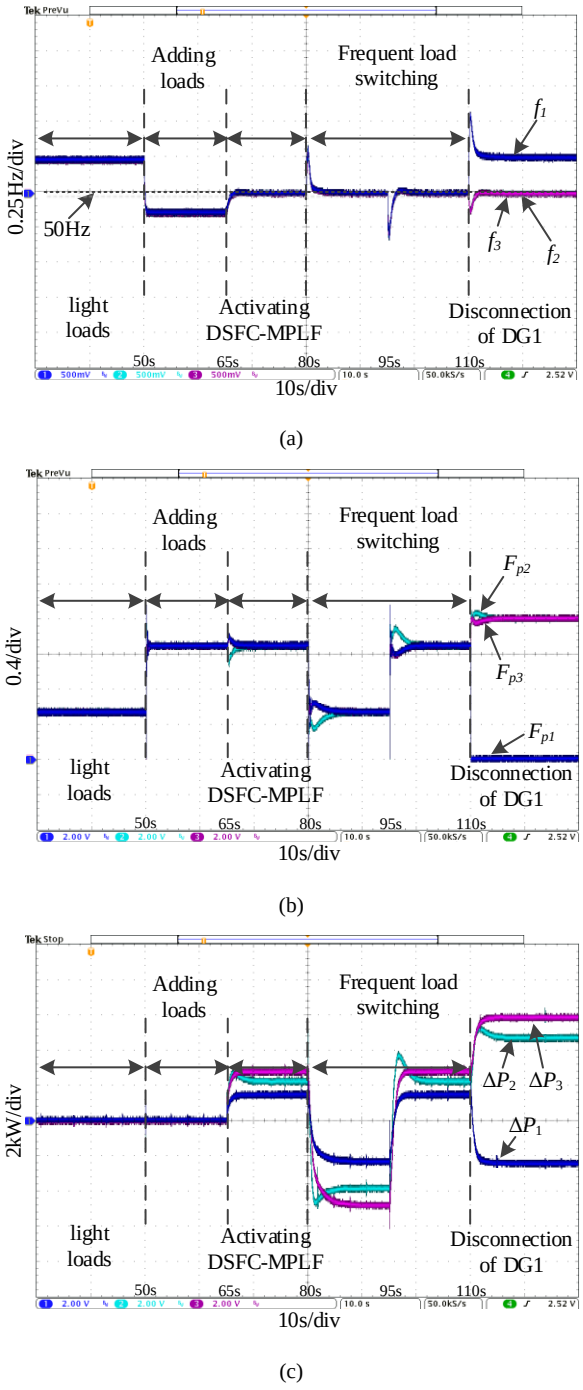

Fig. 17. Performance testing results I of DSFC-MPLF: (a) frequency restoration, (b) output loading factors, (c) compensations for the rated active power with VSG_1 in blue, VSG_2 in green and VSG_3 in purple.

Fig. 17 shows the experiment waveforms in Test I. Fig. 17 (a) shows the system frequency restoration process when loads fluctuate. During the first stage (0 s–50 s), DSFC–MPLF is not employed and the system operates with light loads. The frequency is stable at 50.24 Hz due to the inherent primary control characteristic of VSG. This is slightly higher than the rated value. In the second stage (50 s–65 s), the active-power load increases to 30 kW, which is greater than the rated value. Hence, the system frequency drops to 49.85 Hz, which is slightly lower than the rated value. During the third stage (after 65 s), DSFC–MPLF starts operating. The external PI loop in the secondary-control module of each VSG starts to output

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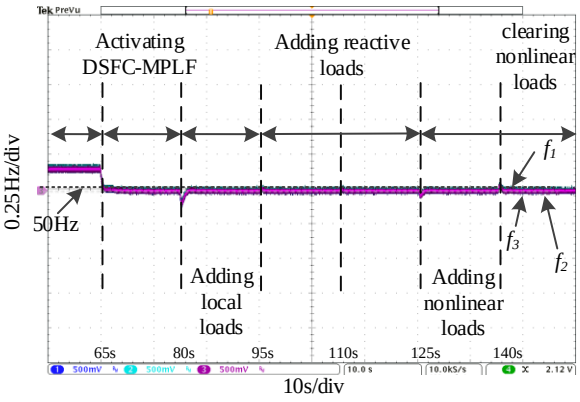
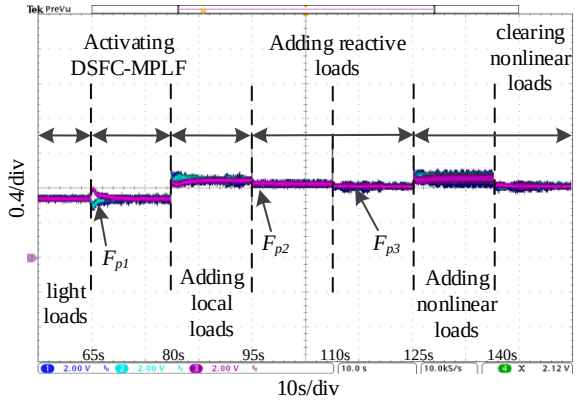
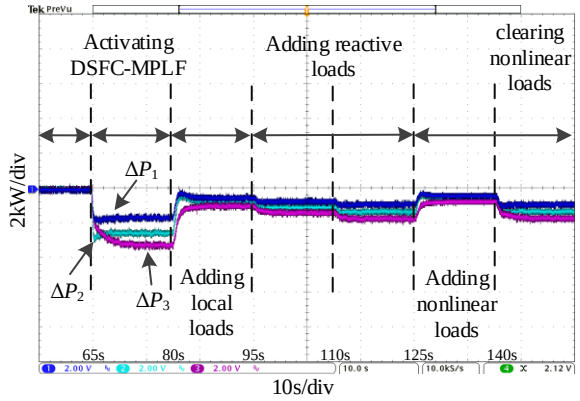


(a)



(b)

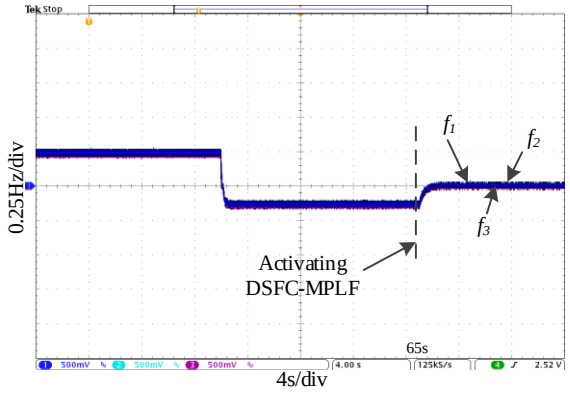


(c)

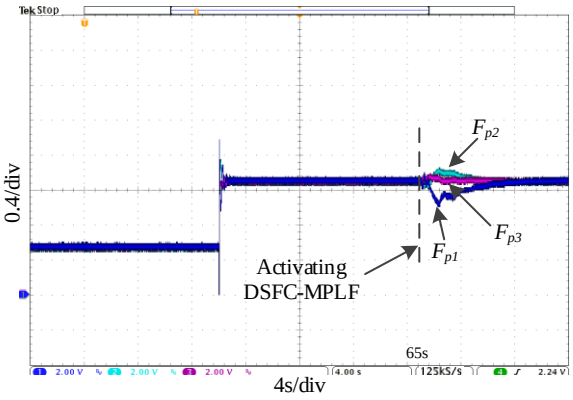
Fig. 18. Performance testing results II of DSFC-MPLF: (a) frequency restoration, (b) output loading factors, (c) compensations for the rated active power with VSG_1 in blue, VSG_2 in green and VSG_3 in purple.

compensations for the local active-power reference to adjust the output of the local VSGs, thereby restoring a system frequency of 50 Hz. In turn, the regulation process is similar when dynamic fluctuations occur (e.g., for t = 80 s, load shedding of 18 kW; for t = 95 s, load loading of 18 kW; for t = 110 s, a VSG_1 exit run occurs). Obviously, no matter how the loads fluctuate, DSFC–MPLF always provides a good SFC performance.

Fig. 17(b) shows the output power waveform, which mainly reflects the power distribution of the three VSGs. From 0 s–65 s, DSFC–MPLF does not operate, and the output factors of each



(a)



(b)

Fig. 19. Performance of DSFC-MPLF for communication latency of 0.2s in VSG_1: (a) frequency restoration, (b) output factors with VSG_1 in blue, VSG_2 in green and VSG_3 in purple.

VSG remain constant under primary control. Owing to the absence of the DSFC–MPLF, the rated power compensations is always zero. At t=65 s, DSFC–MPLF starts to run. It does not affect the power sharing when the system is in the steady state. The VSG-dominated MG can still achieve proportional power sharing with equal output loading factors.

Fig. 17(c) shows the rated active-power compensations for three VSGs. When DSFC–MPLF operates, the active power of the VSGs can be continuously adjusted in approximate accordance with the ratio 5: 8: 10, which indicates that proportional power sharing in the MG has been achieved. Further, it can be observed that even after 110 s, when VSG_1 stops operating, the load can still be redistributed at the rated power ratio of VSG_2 and VSG_3.

The experiment results of Test II are shown in Fig. 18. And frequency fluctuations of the three VSGs under various operating conditions in MGs are described in the Fig. 18 (a). When the proposed method is activated at 65s, the VSG frequency rapidly falls from 50.15 Hz to the rated 50Hz. And during the local load increase by 5kW at 80s, the low power factor addition at 95s, and the non-linear load operation at 125s, the system frequency is always stable around 50Hz, which demonstrates that the proposed SFC method does not affected by MG configurations and load diversities.

The output fluctuations of the three VSGs under various operating conditions in MGs are shown in Fig. 18 (b). When the proposed method is activated at 65s, the outputs from the VSGs

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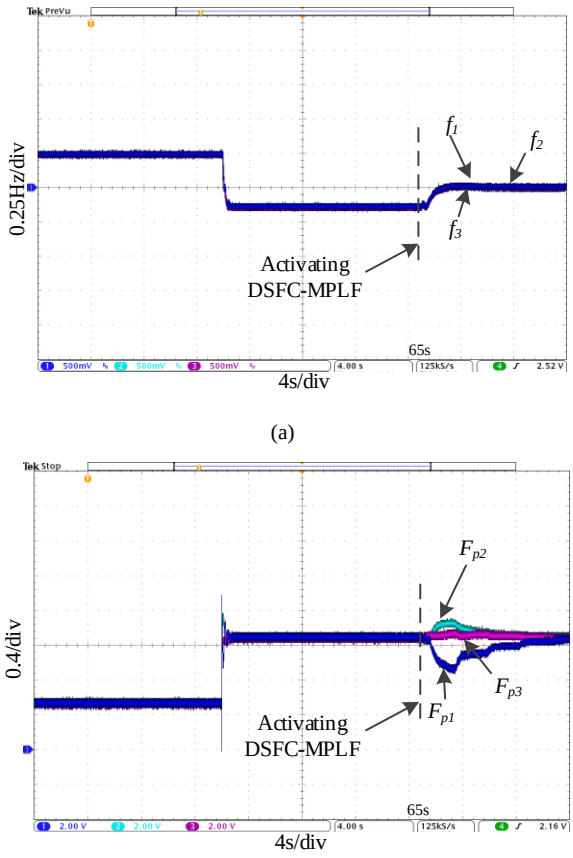

Fig. 20. Performance of DSFC-MPLF for communication latency of 1s in VSG_1: (a) frequency restoration, (b) output factors with VSG_1 in blue, VSG_2 in green and VSG_3 in purple.

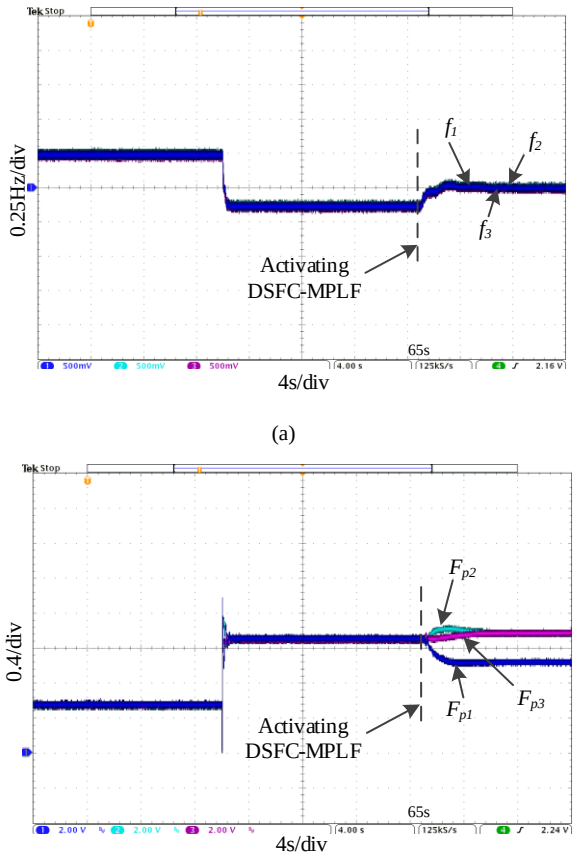

Fig. 21. Performance of DSFC-MPLF when communication in VSG_1 completely fails: (a) frequency restoration, (b) output factors with VSG_1 in blue, VSG_2 in green and VSG_3 in purple.

are equal. During the local load increase at 80s, the low power factor load addition at 110s, and the non-linear load addition at 125s, the power sharing is guaranteed during the whole process except for the switching moment. This proves that the system power sharing under diverse load conditions can be effectively realized by the proposed DSFC-MPLF method.

The active compensation variations for the three VSGs under various operating conditions are depicted in Fig. 18 (c). It can be observed that when the proposed method is applied, the active power compensations are gradually adjusted from 0 to -1.7 kW, -2.6 kW, -3.3 kW, respectively (with the approximate ratio 5.2:8:10.2), which is very close to their rated power ratio (5:8:10). At t = 80s, the increased local load is still distributed among the three inverters according to the rated power capacity. Moreover, after t = 80s, the power compensation ratio is not affected by variations due to the low power factor loads and nonlinear loads.

Based on the analysis above, these experiments effectively verify successful SFC and proportional power sharing functions of the proposed strategy for fluctuating loads, and also verifies the proposed method can operate normally under various operating conditions.

B. Impact of Communication Latency and Failure

These experiments are conducted to demonstrate the impact of the low-bandwidth performance on the system reliability. The communication completely fails and two cases of communication latency in VSG_1 (0.2 s and 1 s, respectively) are compared and discussed. The experimental process of the system is as follows. Initially, the MG operates with a light load of 12 kW and 5 kVar. At 50 s, 18 kW of active load is added as the input. Hence, the total active power changes to 30 kW. At 65 s, DSFC–MPLF starts operating.

As shown in Fig. 19 and Fig. 20, when the proposed strategy is adopted and the communication latency is 0.2 s or 1 s, the VSG-dominated MG can still simultaneously realize the SFC and proportional power sharing under fluctuating loads. Moreover, with increasing time regarding the communication latency, the frequency regulation performance and the power allocation accuracy almost remain unchanged, but the power allocation response becomes slower. This happens mainly for two reasons. Firstly, the SFC function of DSFC–MPLF is automatically implement by the distributed VSG controllers. Secondly, the communication system only transmits a unified reference signal to coordinate the system. When one VSG unit has a long latency, the DDM automatically cancels its qualification regarding the transmission of the output factor.

However, it can still receive F_{pmax} from the communication bus. Therefore, the communication latency can only affect the response speed of power sharing but never its accuracy or the response speed and accuracy of the SFC. Consequently, the system is still able to operate reliably.

Fig. 21 shows the experimental results when the communication system in VSG_1 completely fails. The

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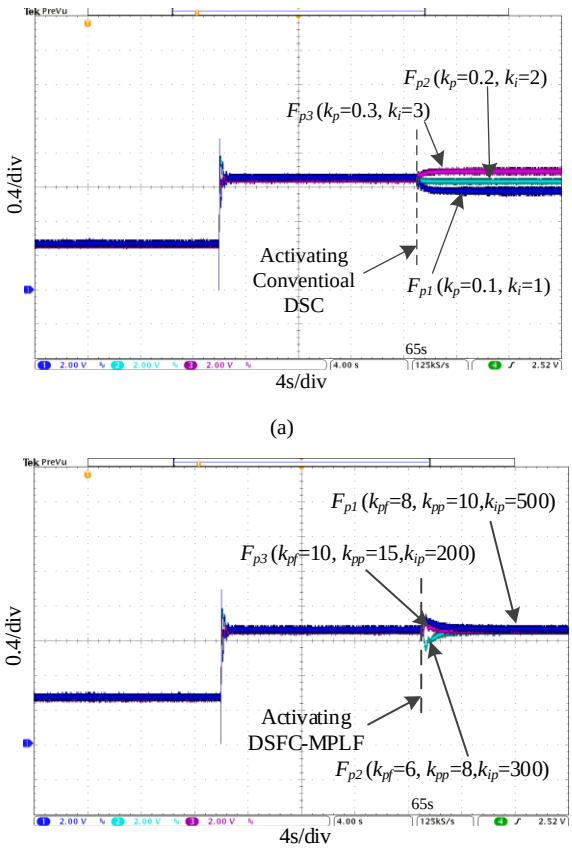

Fig. 22. Output power testing results of conventional DSC strategy and proposed DSFC-MPLF when the three VSGs have different control parameters: (a) output power of conventional DSC strategy, (b) output power of proposed DSFC-MPLF with VSG_1 in blue, VSG_2 in green and VSG_3 in purple.

DSFC–MPLF starts operating at t=65 s. As shown in Fig. 21(a), the system frequency can still quickly recover at 50Hz. Fig. 21(b) illustrates that although VSG_1 cannot output the active power at its rated ratio, it does not affect VSG_2 and VSG_3. This happens because VSG_1 cannot receive the system reference signal and no longer participates in the MPLF grabbing because the communication fails. Thus, it does not affect the system performance.

According to the analysis above, these experiments effectively verify the advantages of low-bandwidth communication and its impact on the SFC and power distribution reliability in MGs.

C. Comparisons with Conventional Strategy

Conventional average-coefficient-based distributed secondary control (DSC) strategies need to collect the complete information of inverters, resulting in heavy communication burdens. Furthermore, it is difficult to coordinate the PI parameter to realize proportional power sharing. In order to highlight the advantages of the proposed strategy regarding these aspects, comparative experiments with the conventional DSC strategy reported in [10] are conducted.

The basic experimental settings in both strategies are the same, except for the PI and P parameters. The k_p value of the three VSGs of the strategy in [10] are 0.1, 0.2, and 0.3; k_i is 1, 2, and 3, respectively. The PI and P parameters of the three VSGs

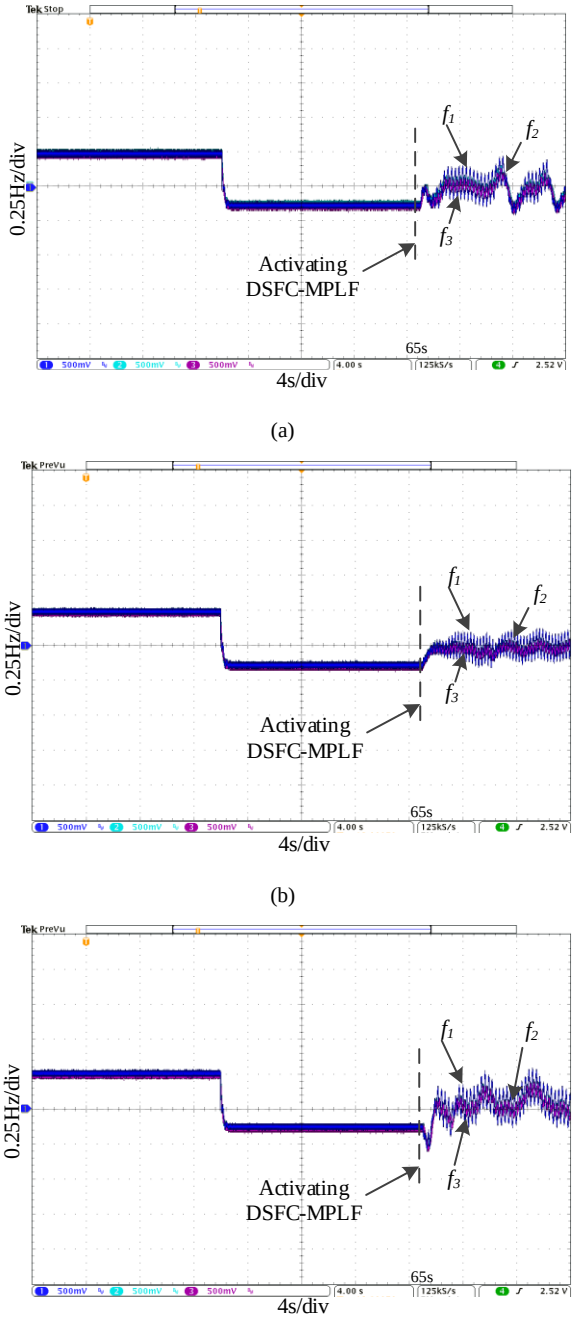

Fig. 23. Frequency of the three VSGs when control parameters in the proposed DSFC-MPLF throughout the stable regions are: (a) k_{pf} = 11, k_{pp} = 10, k_{ip} = 5000, (b) k_{pf} = 8, k_{pp} = 270, k_{ip} = 5000, (b) k_{pf} = 8, k_{pp} = 10, k_{ip} = 7600 with VSG_1 in blue, VSG_2 in green and VSG_3 in purple.

for the proposed strategy are shown in Tab. II. Experimental results are shown in Fig. 22.

As shown in Fig. 22, both strategies are not employed before 65 s. The virtual inertia and droop characteristics of the VSG can easily complete the primary frequency control in the VSG-dominated MG, thereby equalizing the output factors of each VSG unit.

As shown in Fig. 22(a), the conventional DSC strategy is applied after t = 65 s. The output factors of the three VSGs change from the initial ratio 1.3: 1.3: 1.3 to 1.12: 1.28: 1.45. Clearly, although this strategy achieves the SFC, proportional

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power sharing cannot be achieved. This is due to the different PI parameters in the three VSGs. Hence, their frequency compensations are different, resulting in different amplitude changes of the power angles and further forming the circulating current.

According to Fig. 22(b), after t = 65 s and with the proposed strategy, the external communication system continuously provides F_{pmax} in the MG as reference for each VSG. The inner PI loop of each VSG unit continuously compensates its local errors according to the unified reference signal. Not only the SFC is realized, but the output factors of the three VSGs remain stable at a ratio of 1.3: 1.3: 1.3.

Based on the comparison above, these experiments effectively verify the advantages of the proposed strategy regarding power allocation.

D. Validation of Small-Signal Model

In the previous study, the small-signal model of a DSFC–MPLF -based VSG is established, and the stability limits of three PI and P parameters are analyzed. This group of experiments is designed to verify the correctness of the model and to explore the impact of the three parameters on the system stability.

The parameters of VSG_2 and VSG_3 are listed in Tab. II; VSG_1 adopts three new parameter sets, respectively: 1) k_{pp} =10, k_{ip} = 5000, k_{pf} increases from 1–20 with steps of 1; 2) k_{pf} = 8, k_{ip} = 5000, k_{pp} increases from 10–400 with steps of 10; 3) k_{pf} = 8, k_{pp} = 10， k_{ip} increases from 5000–10000 with steps of 100. Initially, the VSG-dominated MG operates with a light load of 12 kW and 5 kVar. At t =50 s, an active power of 18 kW is added. At t =65 s, the DSFC–MPLF is employed. Fig. 23 presents the frequency waveform of the system when the three parameters are increased, respectively.

Fig. 23 (a) shows that for k_{pp} = 10 and k_{ip} = 5000, an oscillatory instability occurs when k_{pf} increases to 11. According to Fig. 23 (b), when k_{pf} = 8 and k_{ip} = 5000, an oscillatory instability occurs when k_{pp} increases to 270. Fig. 23 (c) illustrated that for k_{pf} = 8, k_{pp} = 10, an oscillatory instability occurs when k_{ip} increases to 7700.

Obviously, the stable regions in the experimental results are slightly smaller than those of the theoretical calculation in section III. This is mainly due to two reasons: Firstly, the theoretical calculation adopts ideal values instead of actual values, which differ from each other; Secondly, the mutual influence between VSGs is not considered. The small-signal model in this paper is based on a single VSG, resulting in larger stable regions that in a real situation. However, the stable regions of the experimental and theoretical-model results are consistent in tendency and range. This effectively proves the correctness of the established model and provides some guidance for the optimal design of control parameters.

V. Conclusion

An MPLF-based DSFC strategy has been proposed and verified for islanded MGs containing multiple VSGs. The method can alleviate the limitations of existing distributed secondary control strategies, e.g., a demanding communication system, complex physical implementation, and complex power sharing. The proposed strategy has the following characteristics:

a) Frequency restoration and proportional power sharing in MGs containing multiple VSGs can be achieved simultaneously with the proposed DSFC–MPLF under low-bandwidth communication.

b) When suffering from a VSG breakdown, communication latency, or even failures, the MG is still equipped with an SFC function with fast response speed and high accuracy for a certain time period, i.e., the DSFC–MPLF strategy possesses a high stability and strong robustness.

c) The parameter k_{pf} in the DSFC–MPLF has a small stable region, which mainly affects the performance of power allocation. The parameters k_{pp} and k_{ip} mainly affect the speed and accuracy of a SFC with a relatively larger stable region. In addition, since k_{pf} is in the external control loop, its value should be small. This contrasts with k_{pp} and k_{ip}, which are in the inner PI control loop and whose values should be relatively larger.

APPENDIX

The VSG small signal model is inferred from the following two steps.

Step 1: Disturbance separation and linearization of the time domain equations

From Fig. 7 and Eq. (8), we can obtain the complete VSG control structure and expression, as shown in Eq. (A.1).

$$\begin{cases} T_e = M_f i_f < i, \tilde{\sin}\theta > \\ Q = -\dot{\theta} M_f i_f < i, \tilde{\cos}\theta > \\ \ddot{\theta} = \dfrac{1}{J}(T_m - T_e - D_P\dot{\theta}) \\ e = \dot{\theta} M_f i_f \tilde{\sin}\theta \end{cases} \tag{A.1}$$

Equation (A.2) can be deduced by rewriting the state variables as a sum of steady state and small disturbance.

$$\begin{cases} \dot{\theta} = \dot{\theta}_n + \hat{\dot{\theta}} \\ \delta = \delta_n + \hat{\delta} \\ E = E_n + \hat{E} \\ P_e = P_{en} + \hat{P}_e \\ Q_e = Q_{en} + \hat{Q}_e \end{cases} \tag{A.2}$$

$$\begin{cases} \hat{T}_n - D_p\hat{\dot{\theta}} - \hat{T}_e = J\dfrac{d\hat{\dot{\theta}}}{dt} \\ \hat{Q}_{set} - D_q(\sqrt{2}\hat{E}) - \hat{Q}_e = \sqrt{2}K\dfrac{d\hat{E}}{dt} \\ \hat{\delta} = \int \hat{\dot{\theta}} dt \\ \hat{P}_e = \dfrac{3U_g E_n}{X_s}\hat{\delta} + \dfrac{3U_g}{X_s}\delta_n\hat{E} \\ \hat{Q}_e = \dfrac{3}{X_s}(2E_n - U_g)\hat{E} + \dfrac{3E_n U_g}{X_s}\delta_n\hat{\delta} \end{cases} \tag{A.3}$$

where δ_n, E_n, P_{en} and Q_{en} are the power angle, midpoint voltage effective value, active and reactive output power of the VSG

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during steady-state operation, respectively. $\hat{\theta},\hat{\delta},\hat{E},\hat{P}_e,\hat{Q}_e$ are the small disturbances near stable operating points.

Substituting Eq. (9), (A.2) into Eq. (A.1) and taking the approximation of $\sin\delta_n \approx \delta_n$, $\cos\delta_n \approx 1$, $U_o \approx E$. Eq. (A.3) can be derived by eliminating the DC component on both sides and ignoring the disturbance more than twice [23].

Step 2: Laplacian transform after the linearity of time domain equations

Eq. (A.4) can be obtained by addressing Laplace transform to Eq. (A.3).

$$\begin{cases} \dfrac{\hat{T}_n(s)-\hat{T}_e(s)}{Js+D_p}=\hat{\dot{\theta}}(s) \\ \dfrac{\hat{Q}_n(s)-\hat{Q}_e(s)}{\sqrt{2}(Ks+D_q)}=\hat{E}(s) \\ \hat{\delta}(s)=\dfrac{\hat{\theta}(s)}{s} \\ \hat{P}_e(s)=\dfrac{3U_gE_n}{X_s}\hat{\delta}(s)+\dfrac{3U_g}{X_s}\delta_n\hat{E}(s) \\ \hat{Q}_e(s)=\dfrac{3}{X_s}(2E_n-U_g)\hat{E}(s)+\dfrac{3E_nU_g}{X_s}\delta_n\hat{\delta}(s) \end{cases} \tag{A.4}$$

According to the derivation results in Eq. (A.4), the VSG small signal model is established.

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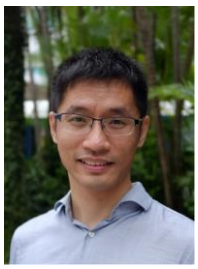

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